USB 2 Channel Digital Amplifier

BU20360

Data Sheet

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TEL:0755-82863877 13242913995 E-MAIL:panxia168@126.com

USB 2 Channel Digital Amplifier

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GENERAL DESCRIPTION

The BU20360 is an integrated single chip of 2-channel pure digital amplifier for USB speaker application. Because no driver is needed for audio playback on all major OS, BU20360 provides a truly plug-and-play feature for external digital audio playback. BU20360 also provide USB suspend mode and resume to save power. To adopt Biforst BPDAT® technology, BU20360 is embedded 2-channel Speaker Driver and 2-channel Earphone Driver with powerful digital audio volume and mute control. It also provides Volume Level Boost function while playing DVD.

FEATURE

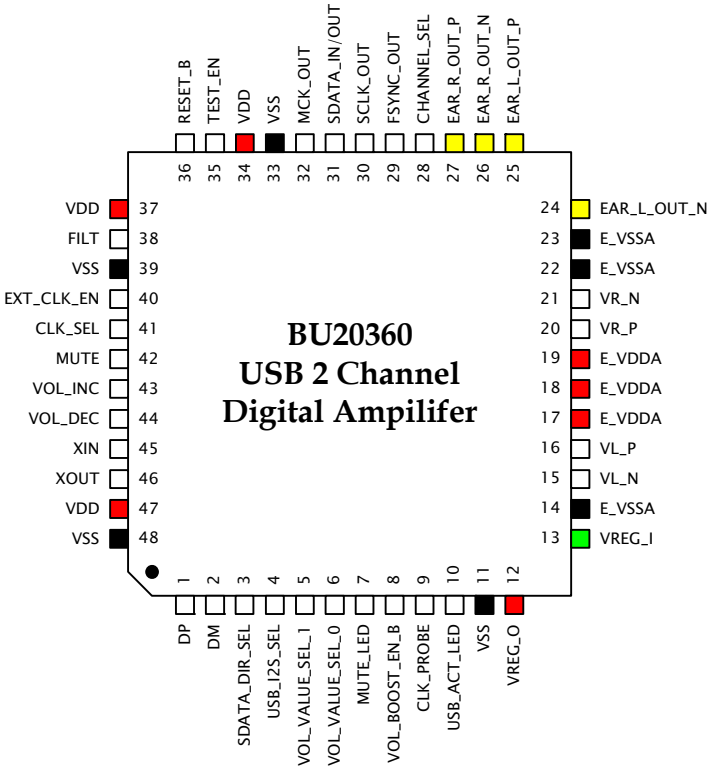
- Certified for Windows Vista x86 / x64
- Works with Windows Vista x86 / x64
- Designed for Windows XP x86 / x64
- Certified by USB-IF
- Fully Compliant with USB 2.0 Full Speed Operation
- Fully Compliant with the USB 1.1 Specification
- Fully Compliant with USB Audio Device Class Specification v1.0
- Fully Compliant with USB HID Device Class Specification v1.1
- USB Bus Powered 500mA Operation with Suspend Mode Support
- Embedded High Performance Digital Amplifier for Speaker & Earphone
- Compatible with Microsoft ™ Windows 98 SE ™ / Windows ME ™ / Windows 2000 / Windows XP ™ / Windows Vista ™ / Apple Mac OS X Without Additional Driver
- Operation Voltage:
  - Digital Part：3.0 ~ 3.6V
  - Speaker & Earphone Driver：3.0 ~ 5.5V
- Operation Frequency:
  - Single 12MHz Crystal Input with On-Chip PLL or Single 48MHz Crystal Input
- Audio Data Input Interface:
  - Can Playback Audio Data From USB (USB Mode)
  - Can Playback Audio Data From I^2S Interface (I^2S Mode)
  - Select Playback From USB or I^2S Interface Through One External Pin
  - I^2S Interface Can Configure At Input Mode or Output Mode (USB to I2S Mode)
- Audio Volume & Mute Control:
  - Provide Separate 32 Level Volume & Mute Control in USB Mode & I^2S Mode
  - Can Set Power-On Initial Volume Value (Only In I^2S Mode)

- Adjust Speaker & Earphone Output Volume Through Two External Pin
- Volume Up, Volume Down & Mute Support USB HID for Host Control Synchronization (Only In USB Mode)
- Provide Volume Boost Function Enable/Disable For Play DVD Movie
- Set Mute Enable/Disable Through External Pin

- Speaker Driver:
  - Embedded 2-Channel Speaker Driver (1W@5V,10%THD at 4Ω Load Per Channel)
  - Embedded 2-Channel Earphone Driver
  - Switch Speaker Driver or Earphone Driver Output Through One External Pin
- LED Indication
  - Provide Mute Enable LED Indication Output
  - Provide USB Active & Receive Audio Data LED Indication Output
- Provide Single 5V External Power Supply With Internal Power Regulation
- Package Type
  - LQFP 48 Pin (7x7x1.4mm)

PIN ASSIGNMENTS, PIN LIST & DESCRIPTION

Pin Assignment



Pin List & Description

Pin No.	Pin	Type	I/O Pad Function
1	DP	Analog (3.3V)	USB Data +
2	DM	Analog (3.3V)	USB Data -
3	SDATA_DIR_SEL	Input (3.3V)	SDATA_IN/OUT (Pin 31) Control Pin *0 : Set SDATA_IN/OUT (Pin 31) at Output Mode* *1 : Set SDATA_IN/OUT (Pin 31) at Input Mode*
4	USB_I2S_SEL	Input (3.3V)	Digital Amplifier Input Audio Data Source Select *0 : Audio Data from USB* *1 : Audio Data from I^2S*
5	VOL_VALUE_SEL_1	Input (3.3V)	Initial Volume Value Select (Audio Data Through I^2S Path Only) *(VOL_VALUE_SEL_1, VOL_VALUE_SEL_0) = 00 : Volume 31* *(VOL_VALUE_SEL_1, VOL_VALUE_SEL_0) = 01 : Volume 16* *(VOL_VALUE_SEL_1, VOL_VALUE_SEL_0) = 10 : Volume 9* *(VOL_VALUE_SEL_1, VOL_VALUE_SEL_0) = 11 : Volume 0*
6	VOL_VALUE_SEL_0		
7	MUTE_LED	Output (3.3V)	Mute Playback Indication LED Output *0 : Mute Playback Disable* *1 : Mute Playback Enable*
8	VOL_BOOST_EN_B	Input (3.3V)	Volume Boost Enable Control *0 : Volume Boost Enable* *1 : Volume Boost Disable*
9	CLK_PROBE	Output (3.3V)	USB Internal Clock Output Probe Point For Debug Use
10	USB_ACT_LED	Output (3.3V)	USB Active Induction LED Output *0 : USB Non-Active* *1 : USB Active* *1 sec Pulse : Digital Amplifier Receive Audio Data From USB*
11	VSS	Power	3.3V Ground Input
12	VREG_O	Power	Internal Regulator Output
13	VREG_I	Power	Internal Regulator Input
14	E_VSSA	Power	Speaker & Earphone Driver Ground Input
15	VL_N	Output (5.0V)	Left Channel Negative PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
16	VL_P	Output (5.0V)	Left Channel Positive PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
17	E_VDDA	Power	Speaker & Earphone Driver 3.3 ~ 5.5V Power Input
18	E_VDDA		
19	E_VDDA		
20	VR_P	Output (5.0V)	Right Channel Positive PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*
21	VR_N	Output (5.0V)	Right Channel Negative PWM Signal Output *(Output Voltage Level Dependent On E_VDDA)*

Pin List & Description

Pin No.	Pin	Type	I/O Pad Function
22	E_VSSA	Power	Speaker & Earphone Driver Ground Input
23	E_VSSA		
24	EAR_L_OUT_N	Output (5.0V)	Left Channel Negative PWM Signal Output for Earphone *(Output Voltage Level Dependent On E_VDDA)*
25	EAR_L_OUT_P	Output (5.0V)	Left Channel Positive PWM Signal Output for Earphone *(Output Voltage Level Dependent On E_VDDA)*
26	EAR_R_OUT_N	Output (5.0V)	Right Channel Negative PWM Signal Output for Earphone *(Output Voltage Level Dependent On E_VDDA)*
27	EAR_R_OUT_P	Output (5.0V)	Right Channel Positive PWM Signal Output for Earphone *(Output Voltage Level Dependent On E_VDDA)*
28	CHANNEL_SEL	Input (3.3V)	Speaker Driver or Earphone Driver Output Enable Select *CHANNEL_SEL = 0 : VL_P/N, VR_P/N Output Enable* *CHANNEL_SEL = 1 : EAR_L_OUT_P/N, EAR_R_OUT_P/N Output Enable*
29	FSYNC_OUT	Output (3.3V)	Serial Audio Data Left/Right Frame Output
30	SCLK_OUT	Output (3.3V)	Serial Audio Data Latch Clock Output
31	SDATA_IN/OUT	Input/Output (3.3V)	Serial Audio Data Input/Output
32	MCK_OUT	Output (3.3V)	12MHz Clock Output for External A/D or Other Device
33	VSS	Power	3.3V Ground Input
34	VDD	Power	3.3V Power Input
35	TEST_EN	Input	Test Mode Enable *0 : Test Mode Disable* *1 : Test Mode Enable*
36	RESET_B	Input (3.3V)	Reset Signal Input *0 : Reset Active (Must Maintain Low Level Great than 1ms)* *1 : Normal Operation*
37	VDD	Power	3.3V Power Input
38	FILT	Analog	PLL External Filter Circuit Connect Path
39	VSS	Power	3.3V Ground Input
40	EXT_CLK_EN	Input (3.3V)	External Clock Input Enable *0 : Internal Crystal OSC Enable* *1 : Use 12MHz or 48MHz Clock to XIN Pin*
41	CLK_SEL	Input (3.3V)	Input Clock Source Frequency Select *0 : 12MHz Clock Source* *1 : 48MHz Clock Source*
42	MUTE	Input (3.3V)	Mute Trigger Signal Input *High Level Trigger Active*
43	VOL_INC	Input (3.3V)	Audio Volume Increase Input *High Level Trigger Active*

Pin List & Description

Pin No.	Pin	Type	I/O Pad Function
44	VOL_DEC	Input (3.3V)	Audio Volume Decrease Input *High Level Trigger Active*
45	XIN	Input (3.3V)	External Clock Input Path or Crystal Connect Point ♦ *EXT_CLK_EN = 0, CLK_SEL = 0 : 12MHz Crystal OSC Input Path* ♦ *EXT_CLK_EN = 0, CLK_SEL = 1 : 48MHz Crystal OSC Input Path* ♦ *EXT_CLK_EN = 1, CLK_SEL = 0 : External 12MHz Clock Input Path* ♦ *EXT_CLK_EN = 1, CLK_SEL = 1 : External 48MHz Clock Input Path*
46	XOUT	Output	12MHz or 48MHz Crystal OSC Output Path
47	VDD	Power	3.3V Power Input
48	VSS	Power	3.3V Ground Input

Function Description

Operation Clock Select

To operate BU20360, it requires an external 12MHz or 48MHz Crystal Oscillator or a direct clock input from of 12MHz or 48MHz thru XIN of pin 45.

The operation clock can be selected thru EXT_CLK_EN of pin 40 and CLK_SEL of pin 41. Table 1 lists the clock, EXT_CLK_EN and CLK_SEL configuration of BU20360. When EXT_CLK_EN is set to Low, BU20360 will use the external Crystal Oscillator as operation clock source. When EXT_CLK_EN is set to High, BU20360 will use the external input clock as source. When CLK_SEL is set to Low, BU20360 is required to connect a 12MHz Crystal Oscillator or 12MHz clock thru XIN. When CLK_SEL is set to High, BU20360 is then required to connect a 48MHz Crystal Oscillator or 48MHz clock thru XIN. Figure 1 shows the recommend application circuit to connect a 12MHz Crystal Oscillator with BU20360. Figure 2 shows the recommend application circuit to connect a 48MHz Crystal Oscillator with BU20360. BU20360 also provides CLK_PROBE of pin 9 to test the internal 48MHz clock is under normal operation or not.

Besides, when EXT_CLK_EN is set to High, XOUT of pin 46 should be floating.

Table 1. BU20360 Operation Clock Configuration

EXT_CLK_EN	CLK_SEL	Input Clock Source Type
0	0	Use One 12MHz Crystal
0	1	Use One 48MHz Crystal
1	0	Use External 12MHz Clock Pulse
1	1	Use External 48MHz Clock Pulse

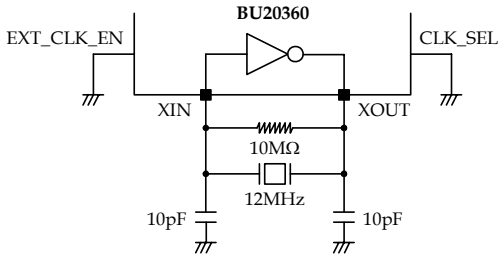


Figure 1. BU20360 Use One 12MHz Crystal Application Circuit

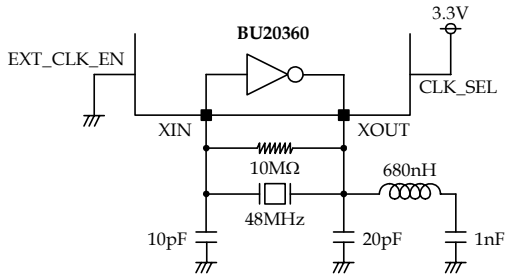


Figure 2. BU20360 Use One 48MHz Crystal Application Circuit

Embedded PLL

BU20360 is embedded a set of PLL to generate the operation clock for internal use. In order to operate PLL normally, it is required to connect FILT of pin 38 with a set of RC circuit to ground. Figure 3 illustrates the recommend application circuit of connect FILT with RC circuit.

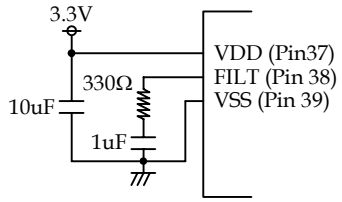


Figure 3. BU20360 FILT (Pin 38) External RC Circuit

Reset

RESET_B pin of BU20360 is the Global Reset for all internal circuit. Table 2 is the setup of RESET_B. When reset BU20360, RESET_B must be set to Low, and remain Low at least 1ms.Then return to High to complete the process of Reset. Therefore, it is recommended to discharge RC in the application circuit and design a simple Power On Reset to stable BU20360 after power on.

Table 2 RESET_B Configuration

RESET_B	BU20360 Status
0	Reset
1	Normal Operation

Volume Boost Enable Configuration

BU20360 provides Volume Boost Enable functions through external pin of DVD_BOOST_EN_B to control enable/disable of Volume Boost. The setups are listed in Table 3.

When VOL_BOOST_EN_B is set to Low, BU20360 will double the output volumes and allow distortion or wow effect. When VOL_BOOST_EN_B is set to High, BU20360 will output the volume in normal mode and automatically eliminate the distortion or wow effect. Therefore, it is highly recommended to set VOL_BOOST_EN_B to Low when play DVD Movie, and set VOL_BOOST_EN_B to High when listening to CD for better performance of auditory sensation.

Table 3. VOL_BOOST_EN_B Configuration

VOL_BOOST_EN_B	Volume Boost Enable
0	Enable
1	Disable

USB Active Indication LED

BU20360 provides an external pin of USB_ACT_LED of pin 10 to connect a LED to indicate the current status of BU20360 receiving USB data. Table 4 lists the configuration of the output of USB_ACT_LED. There are three conditions as stated below.

1. When USB_ACT_LED outputs Low, BU20360 has not yet been completely configured by USB Host. Or USB Host is under Suspend Mode and cannot configure BU20360.
2. When USB_ACT_LED outputs High, BU20360 has been completely configured by USB Host and waiting for the transmission of Audio Data.
3. When Audio Data is transmitted to BU20360, USB_ACT_LED will output the 1 second period pulse.

Table 4. USB_ACT_LED Configuration

USB_ACT_LED	BU20360 Receive USB Data Status
0	USB Configure Non Ready or USB Host In Suspend Mode
1	USB Configure Ready
1 Sec Period Pulse	Receive Audio Data From USB

Digital Amplifier Playback Audio Data Source Select

BU20360 can select playback audio data source from USB or I2S interface. The selection is via external pin of USB_I2S_SEL of pin 4. Table 5 lists the configuration of USB_I2S_SEL. When USB_I2S_SEL is set to Low, BU20360 is under USB Mode and playback the audio data from USB. When USB_I2S_SEL is set to High, BU20360 is under I^2S Mode and playback the audio data from I2S interface.

Table 5. USB_I2S_SEL Configuration

USB_I2S_SEL	Mode Select	Digital Amplifier Playback Audio Data Source Select
0	USB Mode	Playback Audio Data From USB
1	I2S Mode	Playback Audio Data From I^2S Interface

I^2S Audio Data Interface

BU20360 provides a set of I^2S interface to receive the audio data from an external A/D or USB Host. Table 6 lists the configuration of USB_I2S_SEL and SDATA_DIR_SEL. When BU20360 connects an external ADC, SDATA_DIR_SEL must be set to High. Therefore, the Digital Amplifier can select to playback the audio data from USB or ADC thru USB_I2S_SEL. When both USB_I2S_SEL and SDATA_DIR_SEL set to Low, Digital Amplifier will playback the audio data only from USB.

Figure 4 shows the input/output waveform of BU20360 I^2S interface. The external pin of MCK_OUT (Pin 32) will constantly output the clock of 12MHz, SCLK_OUT (Pin 30) output 3MHz and FSYNC_OUT (Pin 29) output 46.875KHz while SDATA_IN/OUT (Pin 31) output or input the data of Left and Right channels.

Table 6. USB_I2S_SEL & SDATA_DIR_SEL Configuration

USB_I2S_SEL	SDATA_DIR_SEL	I^2S Interface Status
0	0	SDATA_IN/OUT (Pin 31) in Output Mode & Output Audio Data from USB Host
0	1	Reserved
1	0	SDATA_IN/OUT (Pin 31) in Output Mode
1	1	SDATA_IN/OUT (Pin 31) in Input Mode & Digital Amplifier Playback Audio Data from I^2S Interface

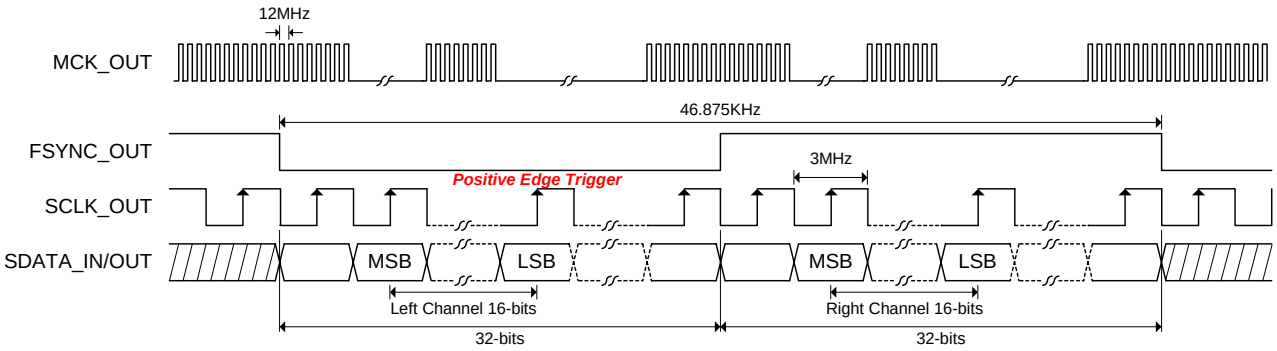


Figure 4. BU20360 I²S Output/Input Waveform

Volume Increase, Decrease & Mute

BU20360 can increase volume via the external pin of VOL_INC (Pin 43), decrease volume via VOL_DEC (Pin 44) and control mute function via MUTE (Pin 42). There are two independent sets of 32-Level volume control built-in BU20360. One can be used when USB_I2S_SEL is set Low (USB Mode) and the other one be used when USB_I2S_SEL is set to High (I²S Mode). The setup of these two sets will not be affected by each other.

When USB_I2S_SEL is set to Low, BU20360 can synchronously volume increase, volume decrease and mute via external pins of VOL_INC, VOL_DEC and MUTE with Windows of PC. When USB_I2S_SEL is set to High, BU20360 can only control the internal Digital Amplifier's functions of volume increase/decrease and mute.

VOL_INC, VOL_DEC and MUTE are to input High Pulse to activate the action. Figure 5 is the Timing Diagram of input signal. The minimum high pulse is 200μs, and so is the interval. When VOL_INC & VOL_DEC set to High over 1 second, BU20360 will auto increase or decrease the volume level.

BU20360 provides external pin of MUTE_LED (Pin 7) to indicate the mute status. Table 7 lists the configuration of MUTE and MUTE_LED. When MUTE_LED output to HIGH, the mute function of Speaker & Earphone Driver is turned on. When MUTE_LED output to LOW, the mute function of Speaker & Earphone Driver is turned off. Further, when mute function is activated and then deactivated, the previous volume value will not be changed.

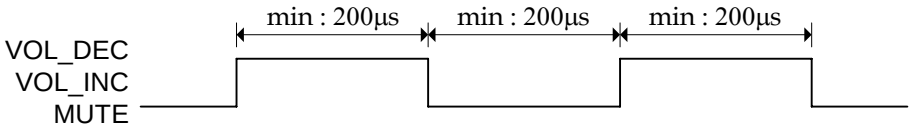


Figure 5. VOL_INC, VOL_DEC & MUTE Control Timing Diagram

Table 7. MUTE & MUTE_LED Configuration

MUTE	MUTE_LED	Mute Control Status
Initial Value	0	Speaker & Earphone Driver Mute Disable
High Pulse (1)	1	Speaker & Earphone Driver Mute Enable
High Pulse (2)	0	Speaker & Earphone Driver Mute Disable

Power-On Initial Volume Configuration

BU20360 provides the function to setup the initial volume value when power-on under I^2S Mode. The setup is via external pins of VOL_VALUE_SEL_0 and VOL_VALUE_SEL_1 to determine the initial volume value. Because the initial volume value under USB Mode is determined by Windows of PC, this setup will not affect the initial volume value of USB Mode.

There are 4 values for setup of BU20360: 0 (Mute)、9、16 and 31 (Max Volume). Table 8 is the corresponding list for setup. Besides, the setup is only valid after reset BU20360.

Table 8. BU20360 Volume Initial Configuration

VOL_VALUE_SEL_1	VOL_VALUE_SEL_0	Initial Volume Value
0	0	31 (Max Volume)
0	1	16
1	0	9
1	1	0 (Mute)

Speaker & Earphone Driver Output Select

BU20360 is embedded one set of Speaker Driver and one set of Earphone Driver. The external pin of CHANNEL_SEL (Pin 28) is used to switch Speaker and Earphone Driver. Table 9 lists the configuration of CHANNEL_SEL. When CHANNEL_SEL is set to Low, BU20360 will output thru Speaker Driver. When CHANNEL_SEL is set to High, BU20360 will output thru Earphone Driver.

Figure 5 illustrates the connection of Speaker and Earphone Driver with Speaker and Earphone. VL_P (Pin 16) and VL_N (Pin 15) are to connect the Speaker of Left channel. VR_P (Pin 20) and VR_N (Pin 21) are to connect the Speaker of Right channel. EAR_L_OUT_P (Pin 25) and EAR_L_OUT_N (Pin 24) are to connect the Earphone of Left channel. EAR_R_OUT_P (Pin 27) and EAR_R_OUT_N (Pin 26) are to connect the Earphone of Right channel.

Further, BU20360 requires Low Pass Filter and the optional circuit in between the Speaker & Earphone Driver and Speaker & Earphone. Please refer to BU20360 Application Note Schematic Drawing for detail Low Pass Filer and optional circuit design.

Table 9. CHANNEL_SEL Configuration

CHANNEL_SEL	Speaker Driver & Earphone Driver Select
0	Speaker Output Enable, Earphone Output Disable
1	Speaker Output Disable, Earphone Output Enable

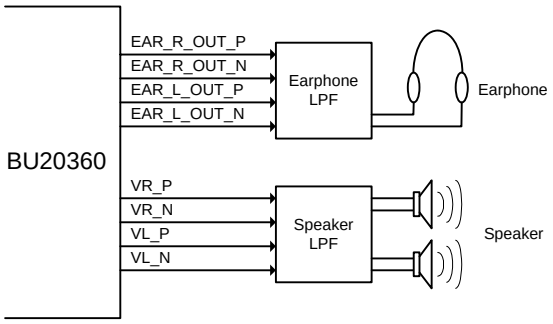


Figure 5. Speaker & Earphone Driver Configuration

Single 5V Power Regulation

BU20360 can use the power directly from USB Port of PC. The power supply from USB is 5.0V 500mA. Figure 6 illustrates how BU20360 built-in Voltage Regulator connects with USB power. BU20360 is required only serial connecting two 1N4148 to external pin of VREG_I (Pin 13) and the 5V power supply from USB and output 3.3V voltage for digital circuits from VREG_O (Pin 12). And also connect VREG_O and VDD (Pin 34, 37, 47), link one 1.5K resist between DP (Pin 1) and VREG_O. Finally connect the 3.3V voltage for circuit controlling VOL_INC, VOL_DEC and MUTE with VREG_O.

If an external 3.3V output Voltage Regulator is used, only connect VREG_O, VREG_I and VDD as shown in Figure 7.

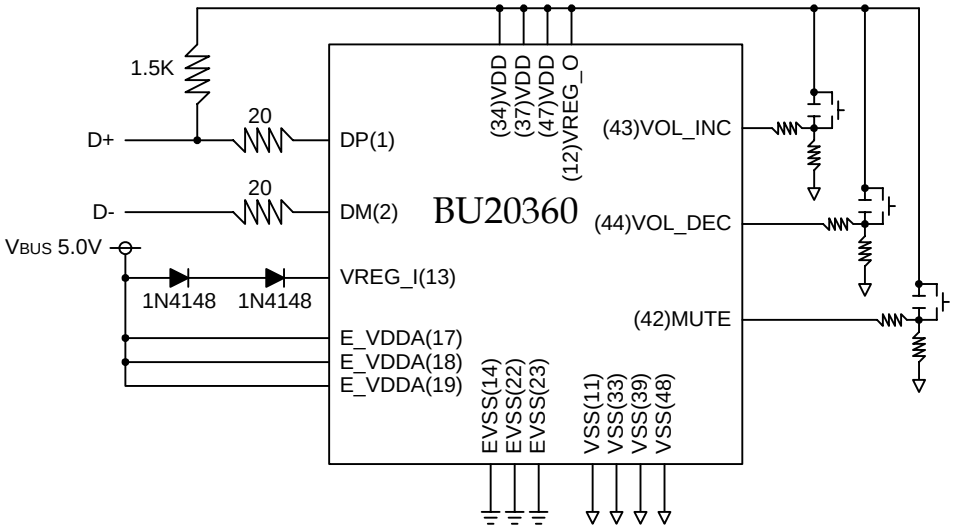


Figure 6. BU20360 Use Internal Voltage Regulator Configuration

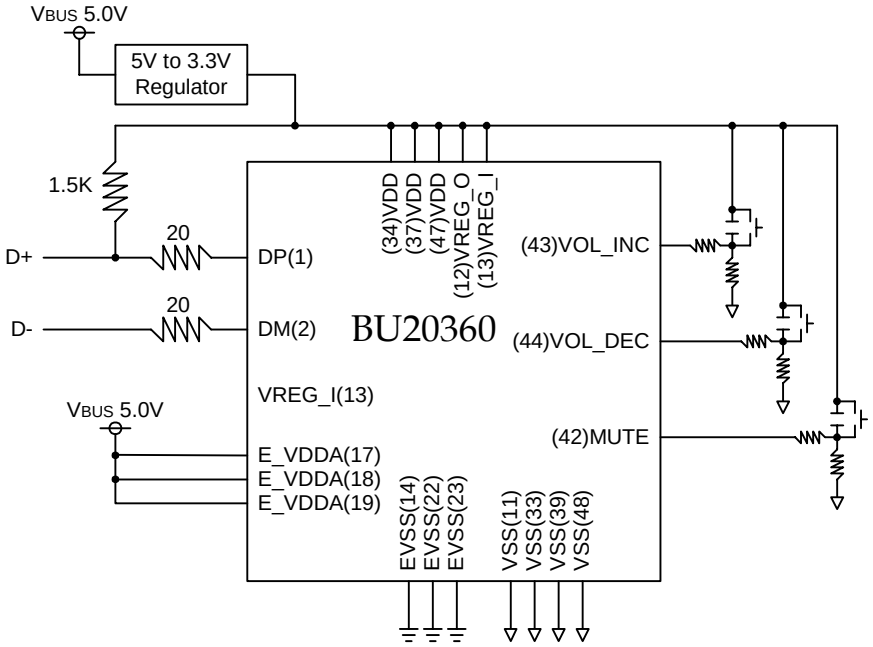


Figure 7. BU20360 Use External Voltage Regulator Configuration

AUDIO PERFORMANCE LIST

Load	Item	Figure Number
3Ω	Frequency Response at 0.25W Output	8
	Frequency Response at 0.5W Output	9
	THD+N VS. Frequency at 0.25W Output	10
	THD+N VS. Frequency at 0.5W Output	11
	THD+N VS. Output Power	12
	Crosstalk at 0.5W Output	13
4Ω	Frequency Response at 0.25W Output	14
	Frequency Response at 0.5W Output	15
	THD+N VS. Frequency at 0.25W Output	16
	THD+N VS. Frequency at 0.5W Output	17
	THD+N VS. Output Power	18
	Crosstalk at 0.5W Output	19
8Ω	Frequency Response at 0.25W Output	20
	Frequency Response at 0.5W Output	21
	THD+N VS. Frequency at 0.25W Output	22
	THD+N VS. Frequency at 0.5W Output	23
	THD+N VS. Output Power	24
	Crosstalk at 0.5W Output	25

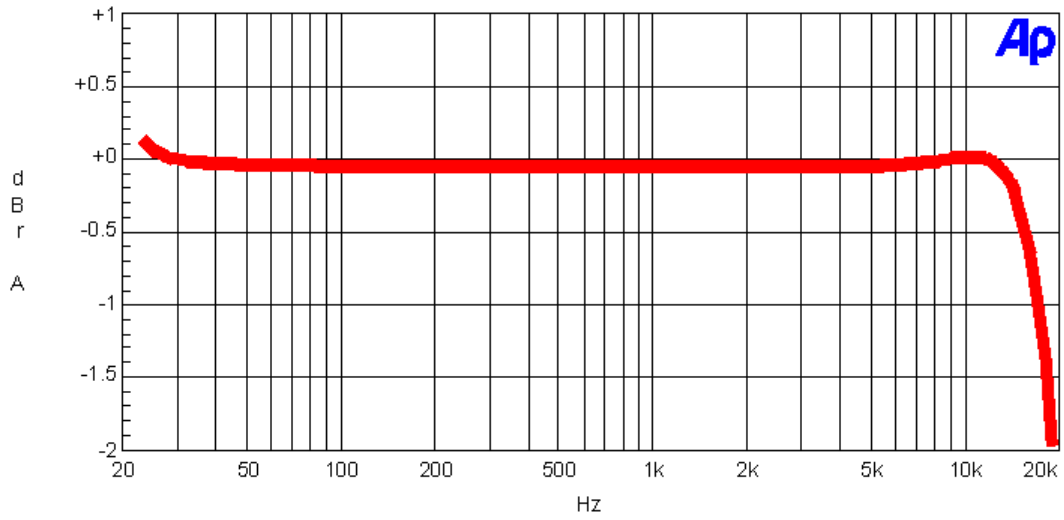


Figure 8. Frequency Response at 3Ω Load, 0.25W Output

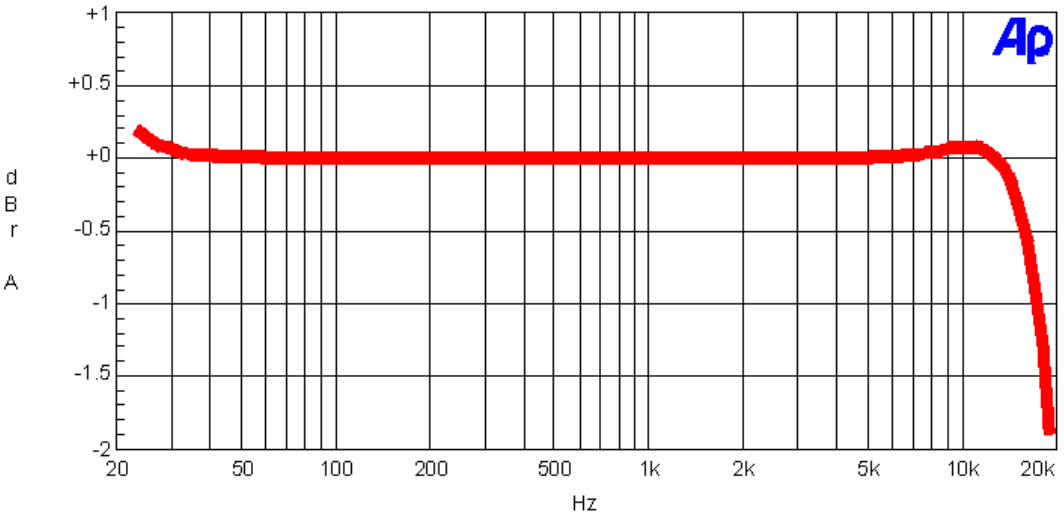


Figure 9. Frequency Response at 3Ω Load, 0.5W Output

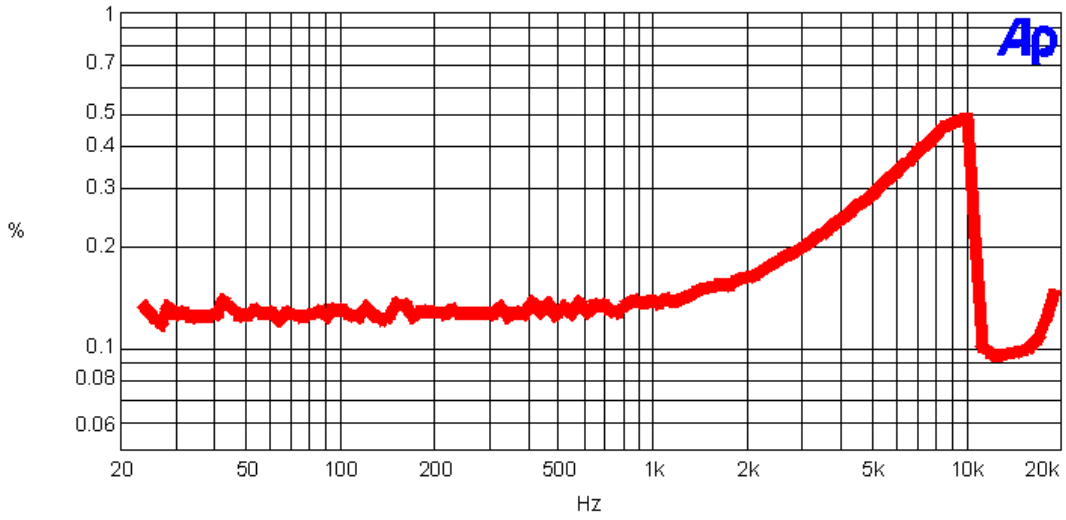


Figure 10. THD+N VS. Frequency at 3Ω Load, 0.25W Output

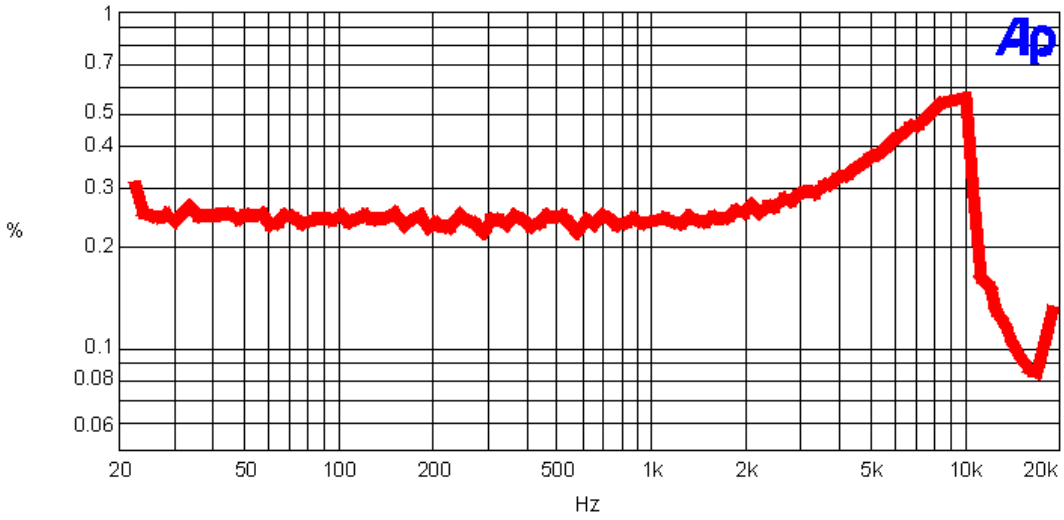


Figure 11. THD+N VS. Frequency at 3Ω Load, 0.5W Output

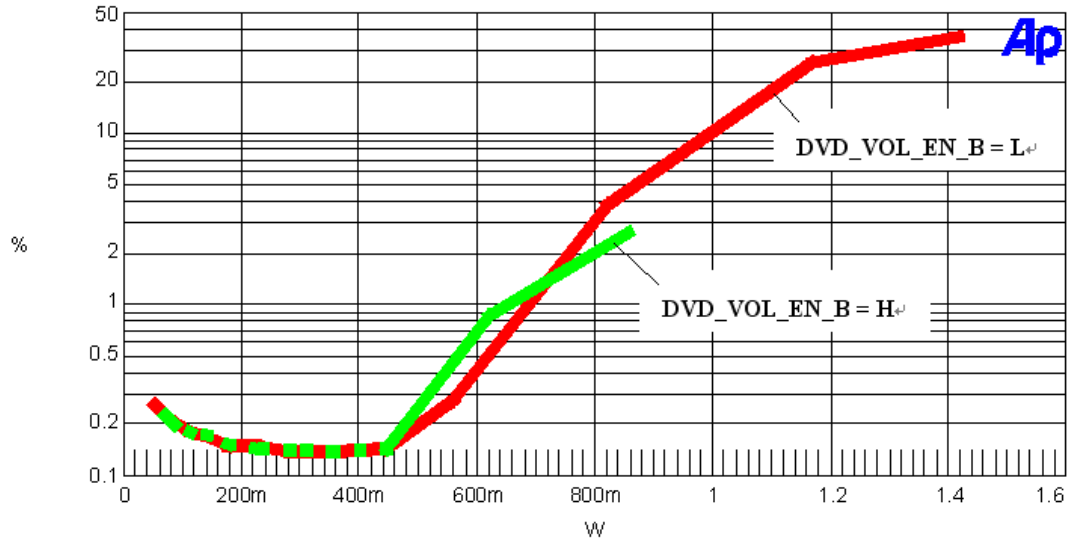


Figure 12. THD+N VS. Output Power at 3Ω Load

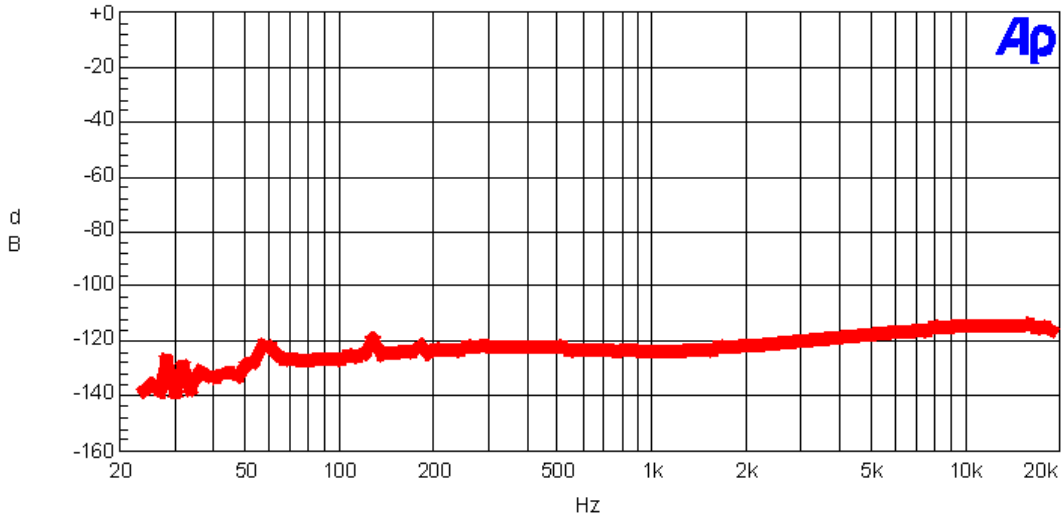


Figure 13. Crosstalk at 3Ω Load, 0.5W Output

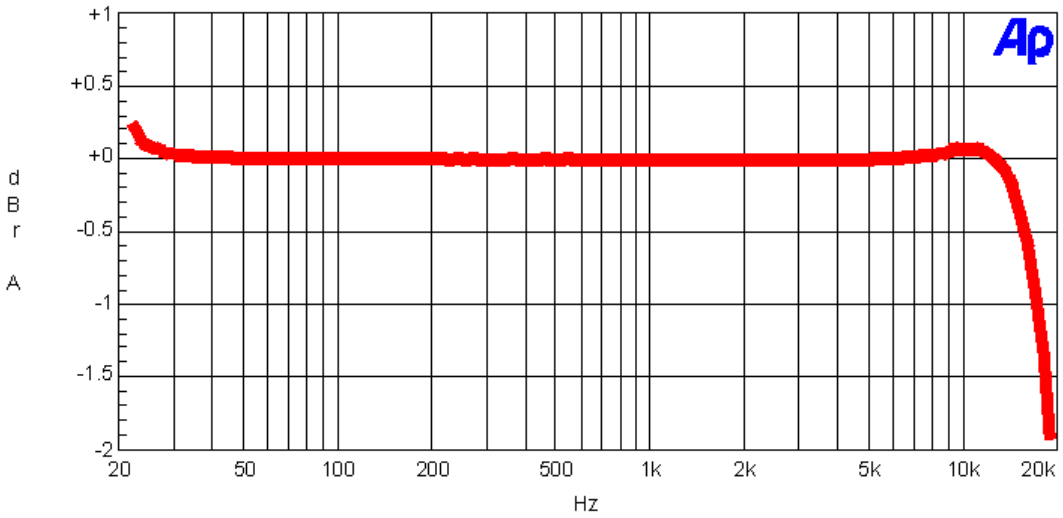


Figure 14. Frequency Response at 4Ω Load, 0.25W Output

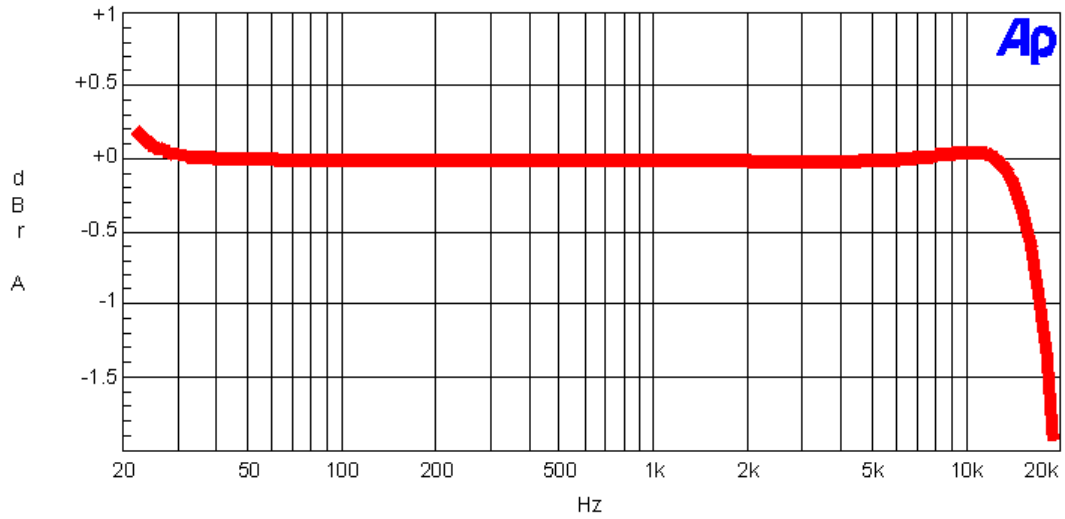


Figure 15. Frequency Response at 4Ω Load, 0.5W Output

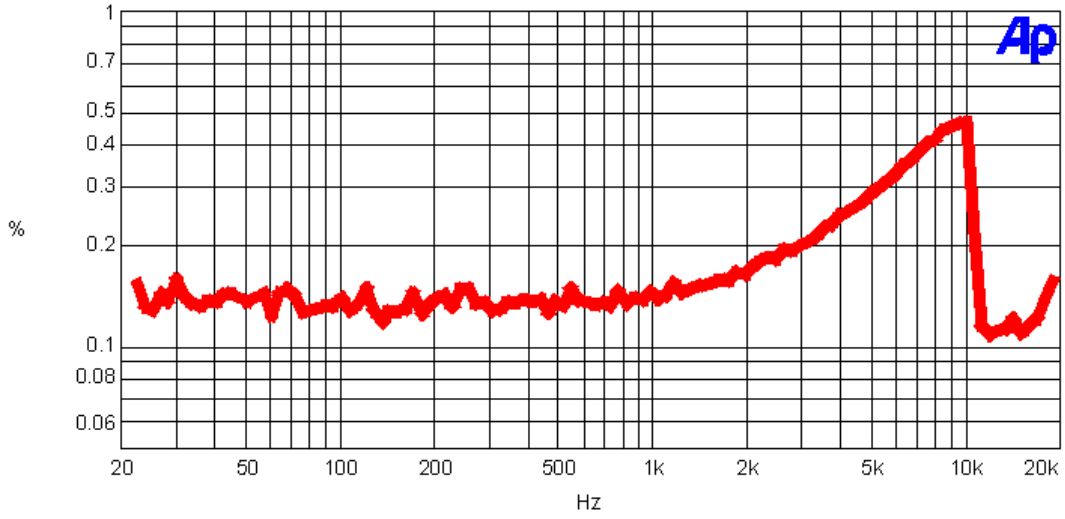


Figure 16. THD+N VS. Frequency at 4Ω Load, 0.25W Output

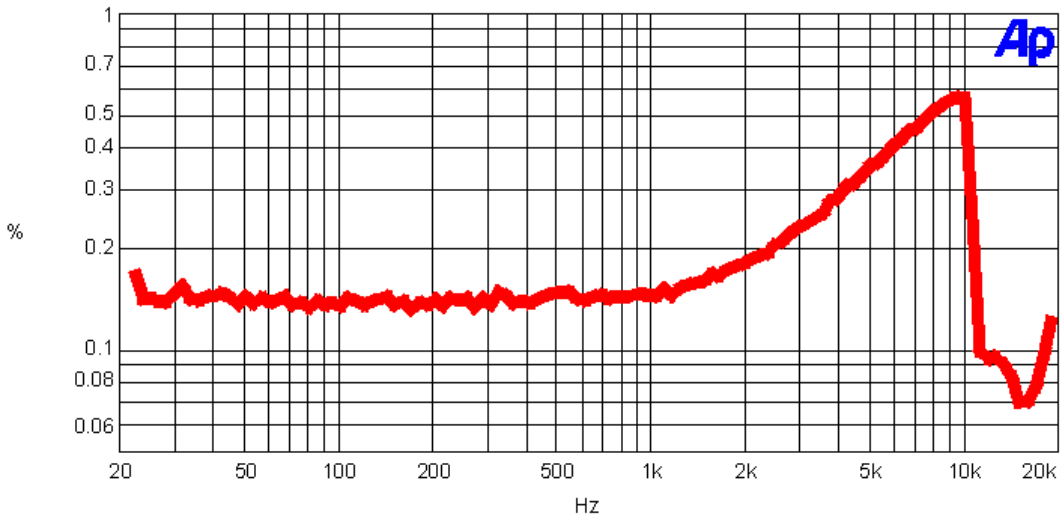


Figure 17. THD+N VS. Frequency at 4Ω Load, 0.5W Output

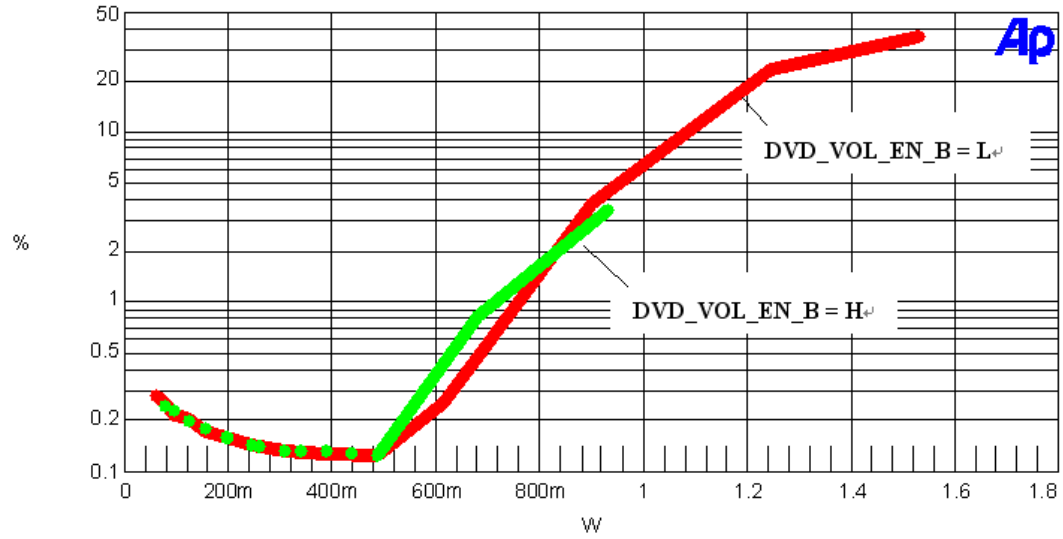


Figure 18. THD+N VS. Output Power at 4Ω Load

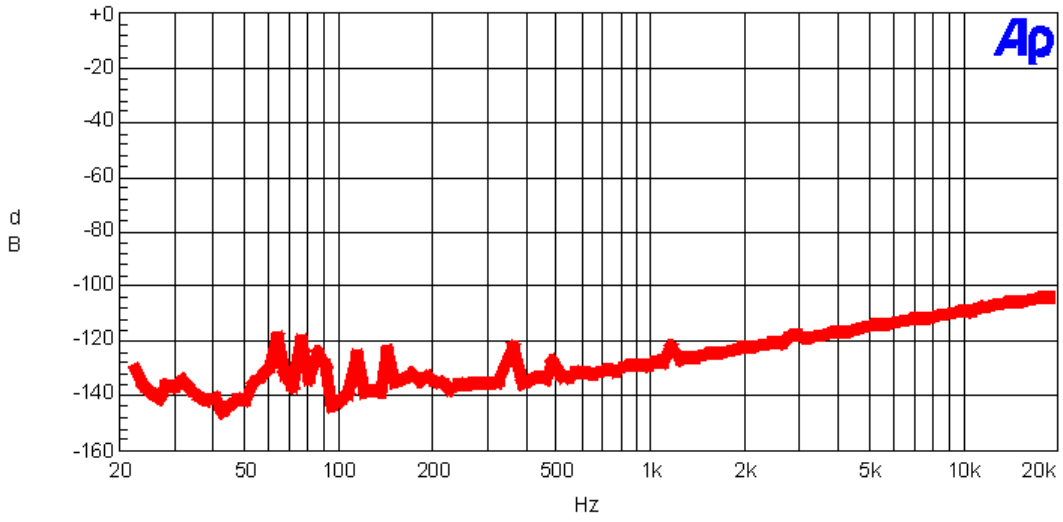


Figure 19. Crosstalk at 4Ω Load, 0.5W Output

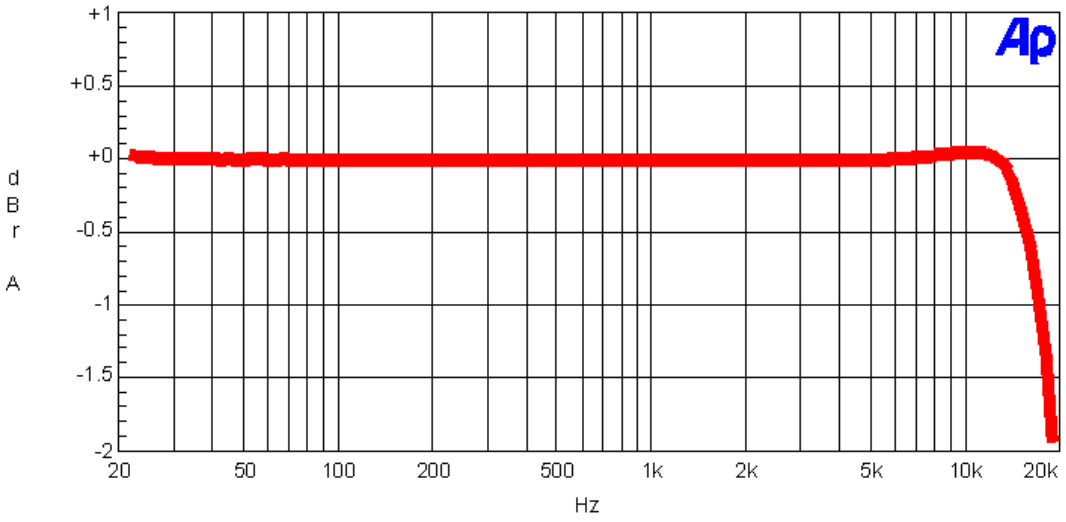


Figure 20. Frequency Response at 8Ω Load, 0.25W Output

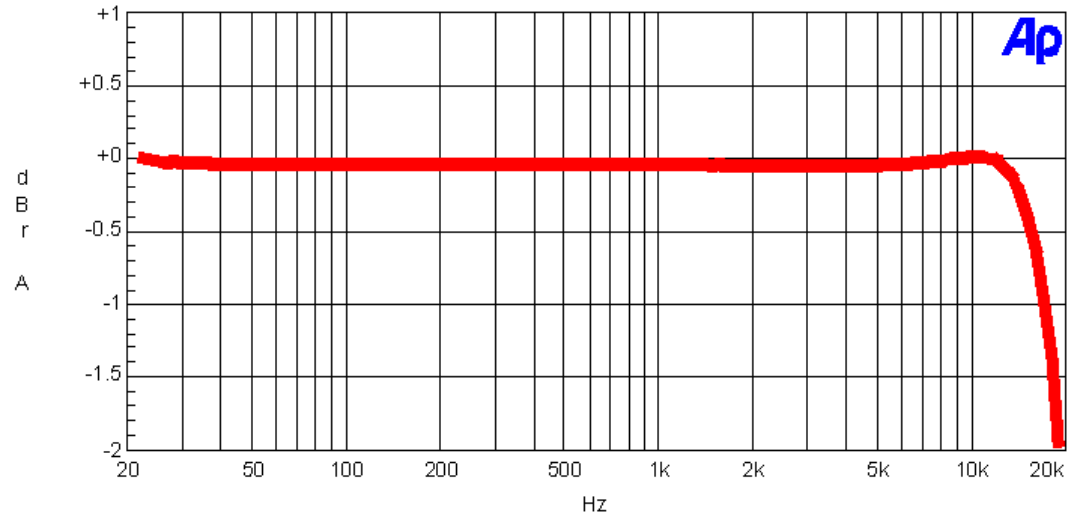


Figure 21. Frequency Response at 8Ω Load, 0.5W Output

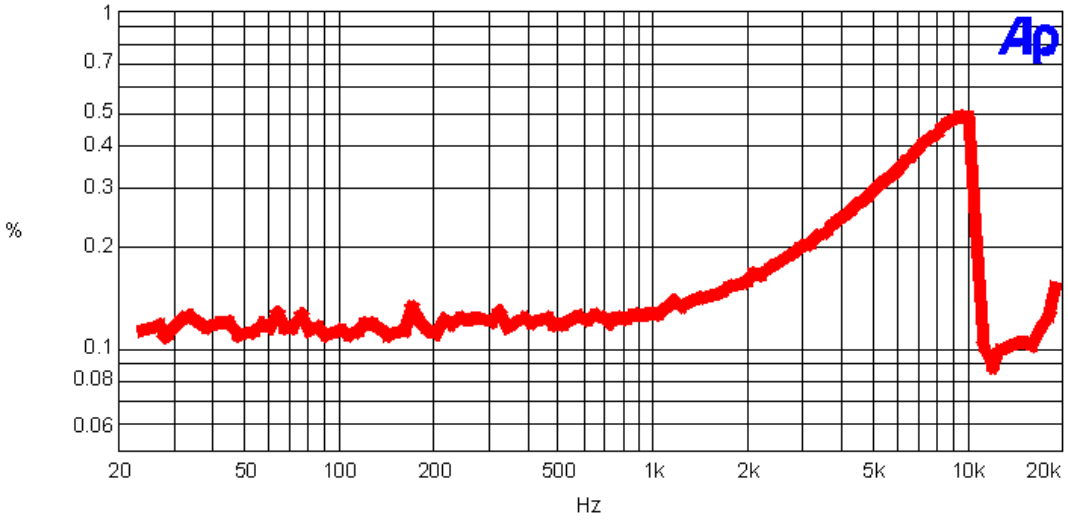


Figure 22. THD+N VS. Frequency at 8Ω Load, 0.25W Output

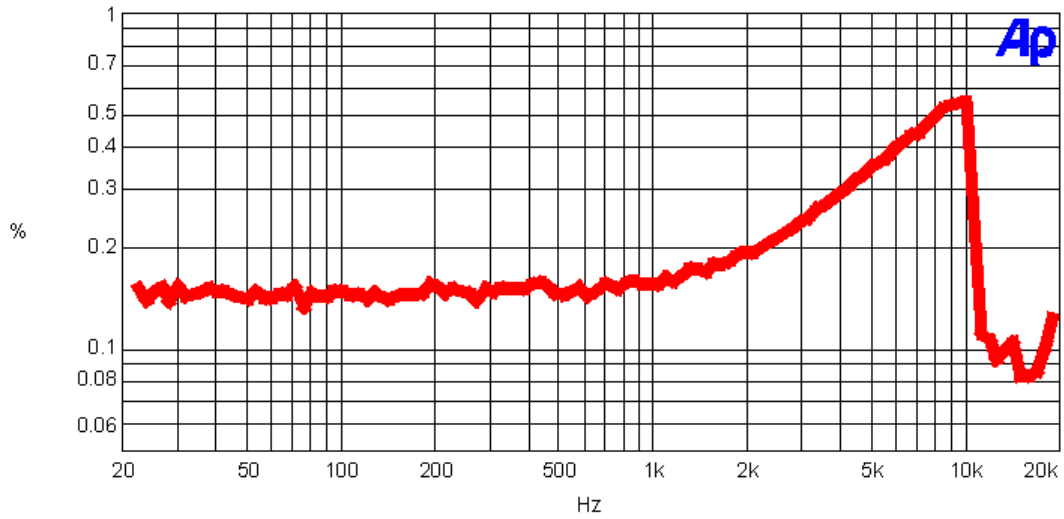


Figure 23. THD+N VS. Frequency at 8Ω Load, 0.5W Output

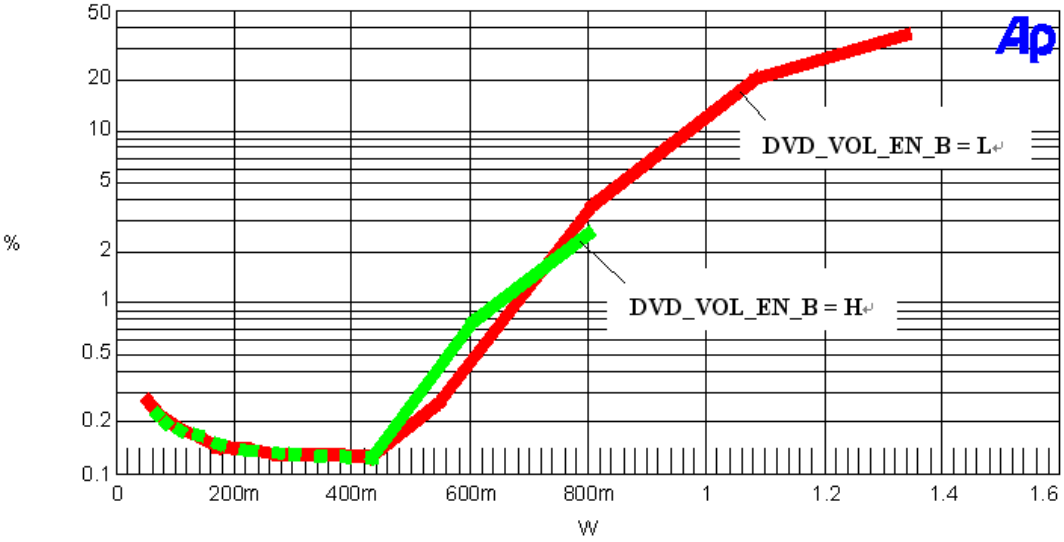


Figure 24. THD+N VS. Output Power at 8Ω Load

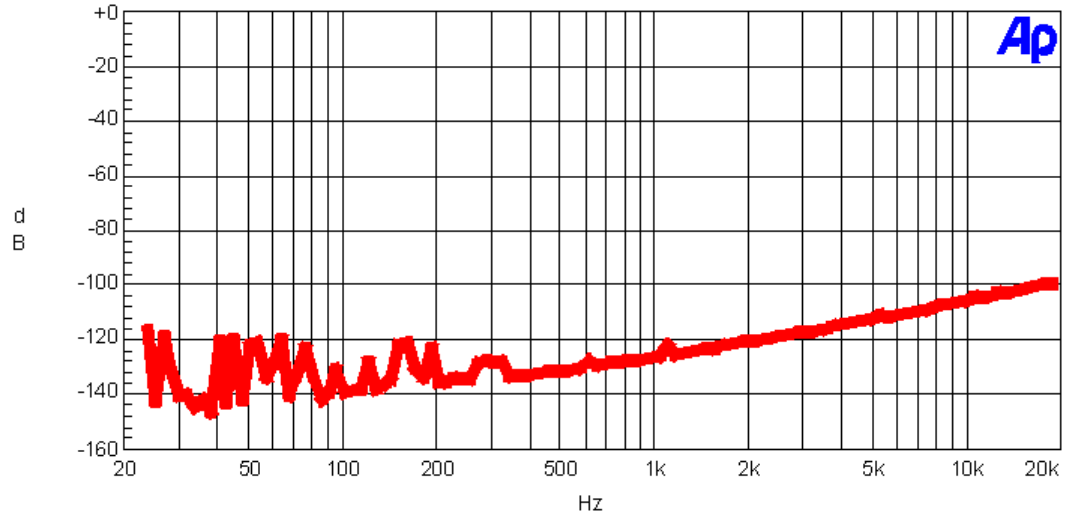


Figure 25. Crosstalk at 8Ω Load, 0.5W Output

Appendix

Biforst Technology has tested and confirmed the following listed operating environments. The BU2036 may work with other PCs and operating systems, but proper operation using them has not been tested and cannot be assured by Biforst Technology.

Operating System

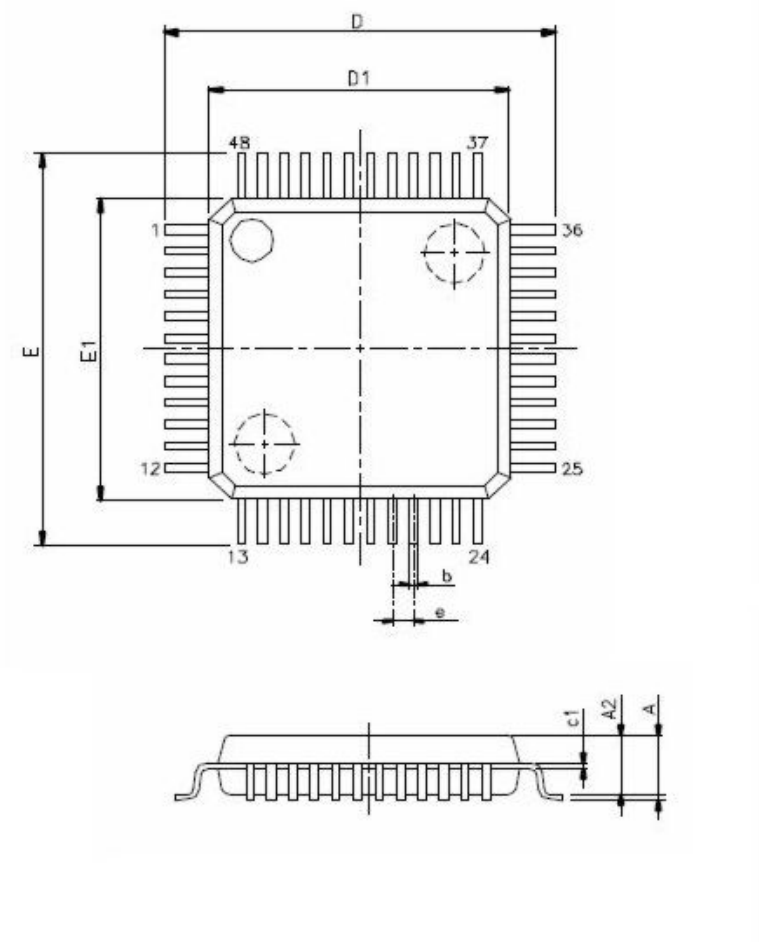
- Microsoft ™ Windows ™ 98SE/Windows ME ™
- Microsoft ™ Windows 2000 Professional
- Microsoft ™ Windows XP ™ Home/Professional with Service Pack 1 or Service Pack 2
- Microsoft ™ Windows Vista All Series
- Mac OS X 10.4

PC-AT Compatible Computer Running A Listed OS (OS Requirement Must Be Met)

- Motherboard Use ATI Radeon 9100IGP & ATI IXP200 (USB Controller in the Chipset)
- Motherboard Use Intel 815E & Intel 82801BA (USB Controller in the Chipset)
- Motherboard Use Intel 830MP & Intel 82801CAM (USB Controller in the Chipset)
- Motherboard Use Intel 845D & Intel 82801BA (USB Controller in the Chipset)
- Motherboard Use Intel 845G & Intel 82801DB (USB Controller in the Chipset)
- Motherboard Use Intel 865P/PE/G & Intel 82801EB (USB Controller in the Chipset)
- Motherboard Use Intel 915P/G & Intel 82801FB (USB Controller in the Chipset)
- Motherboard Use SIS 661FX & SIS 964 (USB Controller in the Chipset)
- Motherboard Use SIS ID065 & SIS LPC Bridge (USB Controller in the Chipset)
- Motherboard Use ULI M1683 & ULI M1563 (USB Controller in the Chipset)

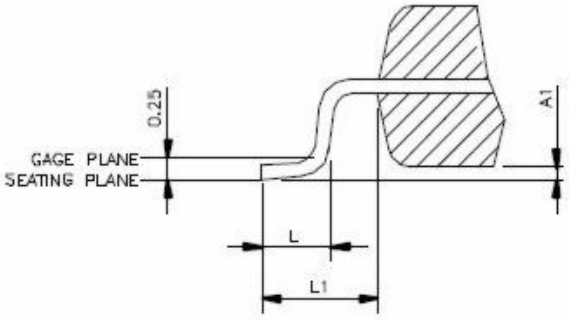
PACKAGE DIMENSION

LQFP48



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	——	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	



Version History

Version	Date	Page	Description
1.0	2005.11.16		First Release
1.1	2007.07.01		Add Feature List & Audio Performance