TA8803

3W Filterless Stereo Class-D Audio Amplifier with Digital Volume Control

Key Features

3W Output at 10% THD with a 4Ω Load and 5V Power Supply
Filterless, Low Quiescent Current and Low EMI
Low THD+N
64-step Digital Volume Control
Superior Low Noise
Low pop noise
Efficiency up to 90%
Short Circuit Protection
Thermal Shutdown
Few External Components to Save Space and Cost
Pb-Free Package

General Description

The TA8803 is a 3W, class-D audio amplifier with 64-step digital volume control. It offers low THD+N, allowing it to produce high-quality sound reproduction. The new filterless architecture allows the device to drive the speaker directly, without needing low-pass output filters, which will save 30% system cost and 75% PCB area.

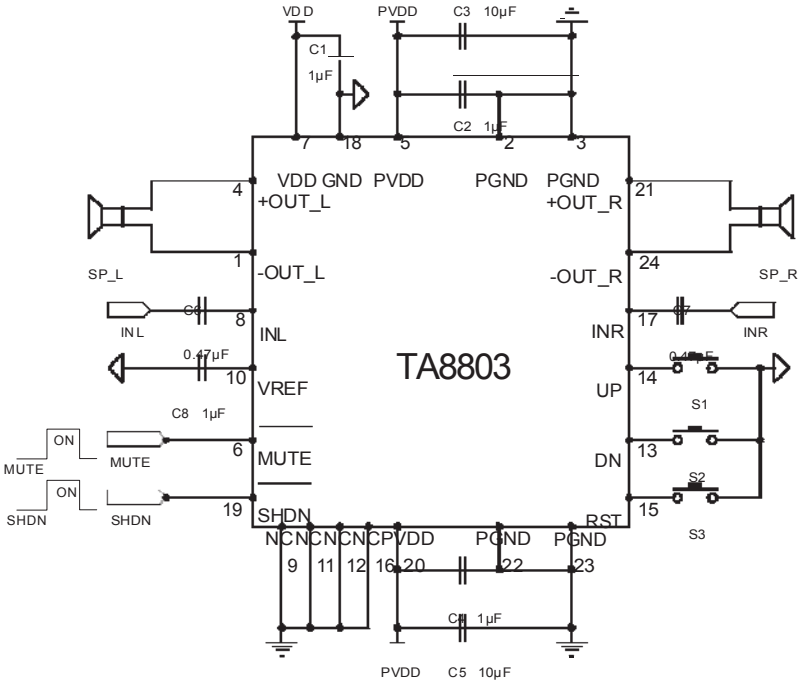
With the same numbers of external components, the efficiency of the TA8803 is much better than class-AB cousins. It can extend the battery life, ideal for portable applications.

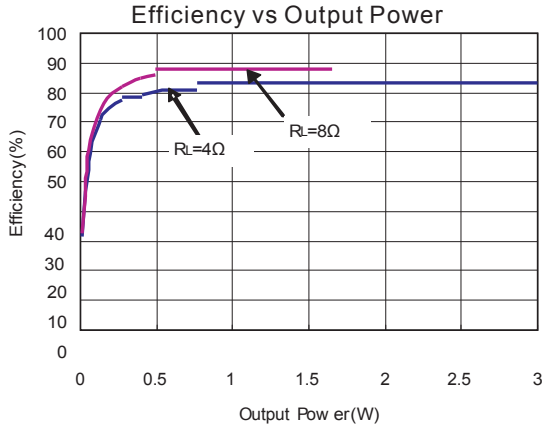
The TA8803 is available in a SSOP-24 package.

Applications

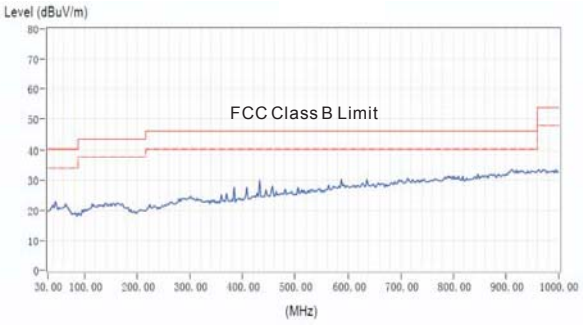
LCD Monitors/TV Projectors
Notebook Computers
Portable Speakers
Portable DVD Players, Game Machines
Cellular Phones/Speaker Phones

Typical Application





Radiated Emissions



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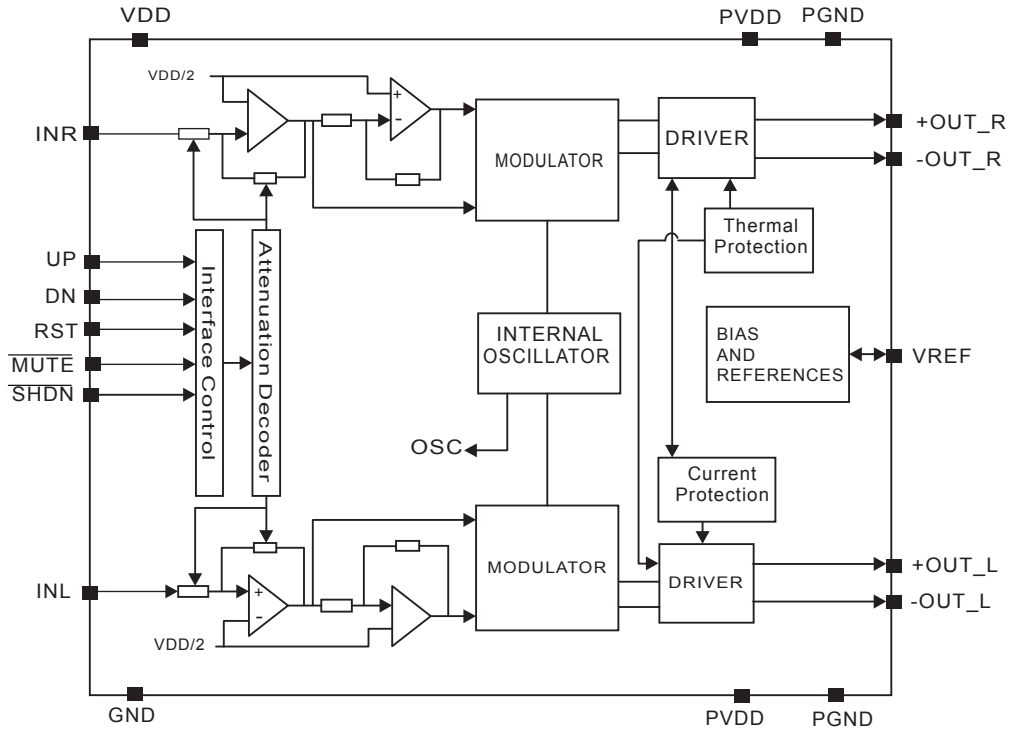
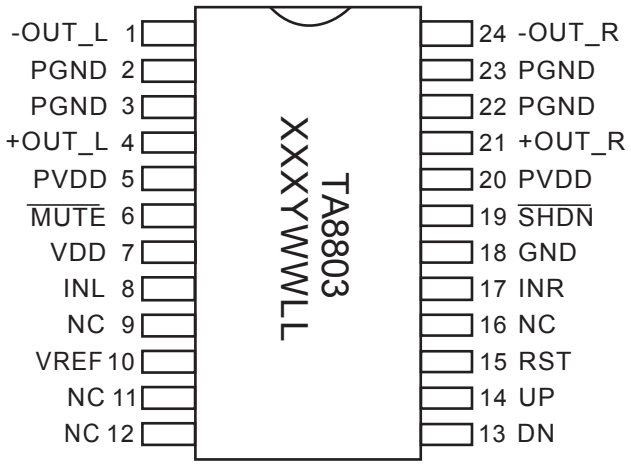
05/2010

Block Diagram



Pin Configuration & Marking Information

Top View
SSOP-24



X: Internal Code
Y: Year
WW: Week
LL: Internal Code

Pin Descriptions

Pin Number	Pin Name	Description
1	-OUT_L	Left Channel Negative Output
2	PGND	Power GND
3	PGND	Power GND
4	+OUT_L	Left Channel Positive Output
5	PVDD	Power VDD
6	$\overline{\text{MUTE}}$	Mute Control Input（active low）, pull-up
7	VDD	Analog VDD
8	INL	Left Channel Input
9	NC	No Connect
10	VREF	Internal analog reference, connect a bypass capacitor from VREF to GND
11	NC	No Connect
12	NC	No Connect
13	DN	Volume down Control (active low)
14	UP	Volume up Control (active low)
15	RST	Volume Controller Reset (active low)
16	NC	No Connect
17	INR	Right Channel Input
18	GND	Analog GND
19	$\overline{\text{SHDN}}$	Shutdown Control Input(active low), pull-down
20	PVDD	Power VDD
21	+OUT_R	Right Channel Positive Output
22	PGND	Power GND
23	PGND	Power GND
24	-OUT_R	Right Channel Negative Output

Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Supply Voltage at no Input Signal.....6.0V
Input Voltage.....-0.3V to V_{DD}+0.3V
Maximum Junction Temperature.....150°C
Storage Temperature.....-65°C to 150°C
Soldering Temperature.....300°C, 5sec

Recommended Operating Conditions

Supply voltage Range.....2.2V to 5.5V
Ambient Temperature Range.....-40°C to 85°C
Junction Temperature Range.....-40°C to 125°C

Thermal Information

Parameter	Symbol	Package	Maximum	Unit
Thermal Resistance (Junction to Ambient)	θ_{JA}	SSOP-24	96	°C/W

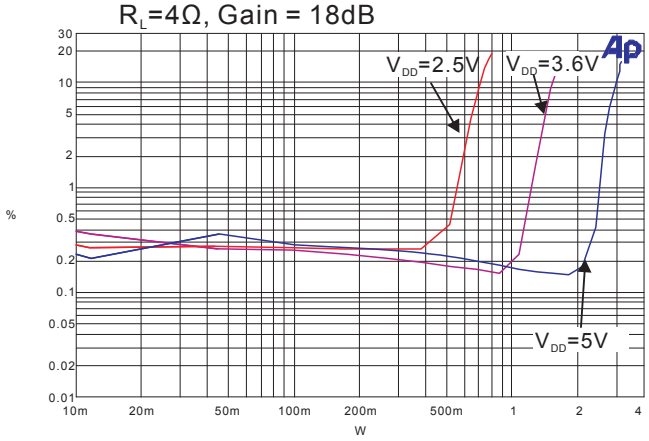
Electrical Characteristic

V_{DD}=5V, Gain = 18dB, R_L=8Ω, T_A=25°C, unless otherwise noted.

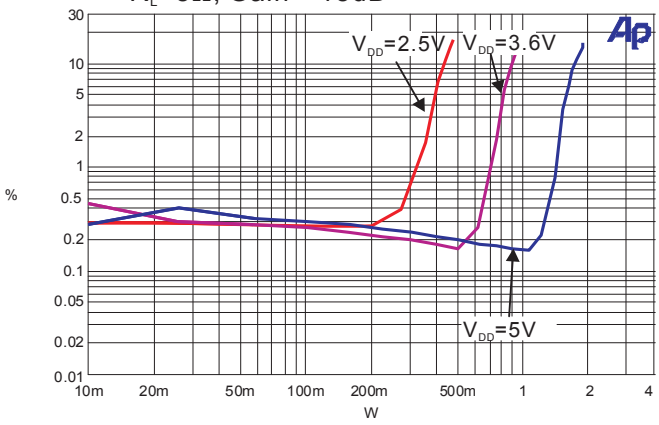
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}			2.2		5.5	V
Quiescent Current	I_Q	No Load			7	15	mA
		R_L=8Ω			8		
		R_L=4Ω			8.5		
Mute Current	I_{MUTE}	V_{MUTE}=0V			2.5	4	mA
Shutdown Current	I_{SHDN}	V_{SHDN}=0V			0.5	10	μA
$\overline{SHDN}$ Input High	V_{SH}			1.2			V
$\overline{SHDN}$ Input Low	V_{SL}					0.5	
$\overline{MUTE}$ Input High	V_{MH}			1.2			V
$\overline{MUTE}$ Input Low	V_{ML}					0.5	
Output Offset Voltage	V_{OS}	No Load			120	300	mV
Drain-Source On-State Resistance	$R_{DS(ON)}$	I_{DS}=0.5A	P MOSFET		0.3	0.40	Ω
			N MOSFET		0.22	0.35	
Output Power	P_O	f=1kHz	R_L= 8Ω,THD=1%	1.1	1.3		W
			R_L= 8Ω,THD=10%	1.5	1.7		
			R_L= 4Ω,THD=1%	1.9	2.1		
			R_L= 4Ω,THD=10%	2.8	3.0		
Total Harmonic Distortion Plus Noise	THD+N	R_L=8Ω, P_O=0.5W			0.19		%
		R_L=8Ω, P_O=1.0W			0.22		
		R_L=4Ω, P_O=1.0W			0.17		
		R_L=4Ω, P_O=2.0W			0.25		
Power Supply Ripple Rejection	PSRR	No input, f=1kHz, Vpp=200mV		45	55		dB
Channel Separation	CS	P_O=1W, R_L=4Ω		60	80		dB
Oscillator Frequency	f_{OSC}				250		kHz
Efficiency	η	P_O=1.7W, f=1kHz, R_L=8Ω		85	89		%
		P_O=3.0W, f=1kHz, R_L=4Ω		80	83		%
Signal Noise Ratio	SNR	f =22 to 22kHz, THD=1%	R_L=4Ω		85		dB
			R_L=8Ω		87		dB
Under Voltage Lock-out	UVLO				1.95		V
Over Temperature Protection	OTP				150		°C
Over Temperature Hysteresis	OTH				60		°C

Typical Operating Characteristics (T_A=25°C)

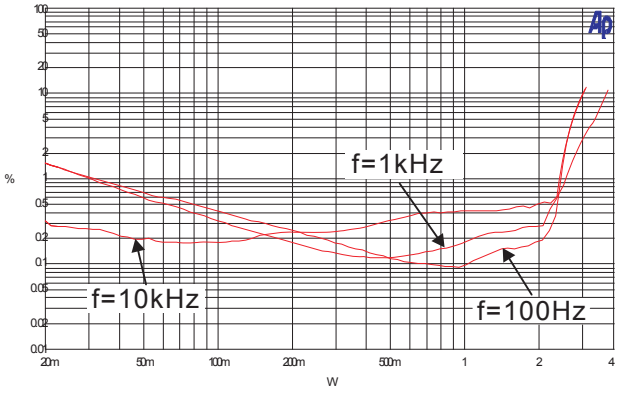
1. THD+N vs Output Power
R_L=4Ω, Gain = 18dB



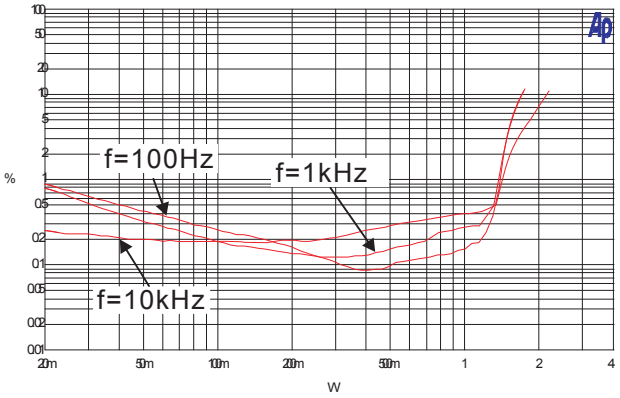
2. THD+N vs Output Power
R_L=8Ω, Gain = 18dB



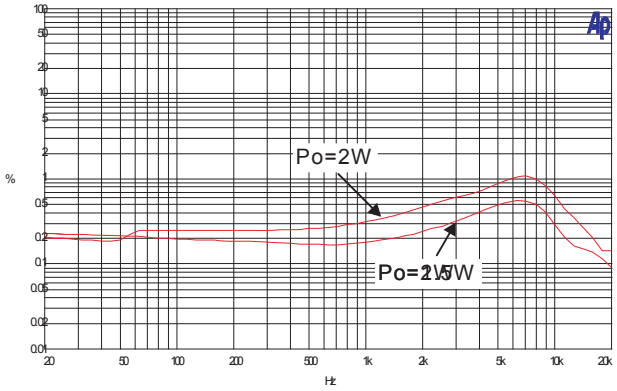
3. THD+N vs Output Power
V_{DD}=5V, R_L=4Ω, Gain = 18dB



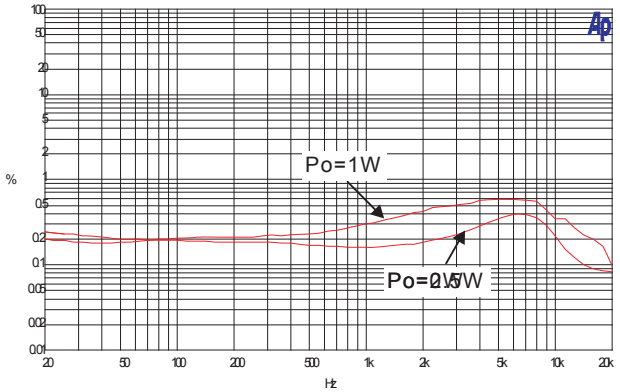
4. THD+N vs Output Power
V_{DD}=5V, R_L=8Ω, Gain = 18dB



5. THD+N vs Frequency
V_{DD}=5V, R_L=4Ω, Gain = 18dB

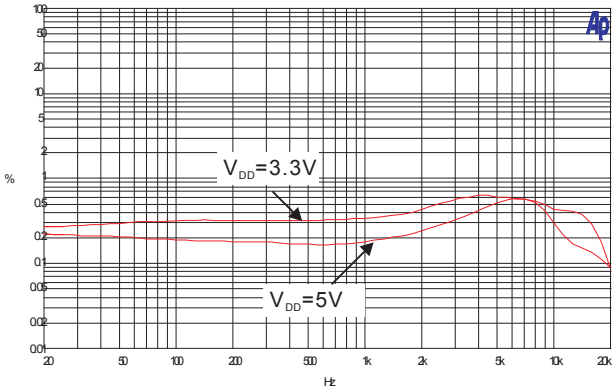


6. THD+N vs Frequency
V_{DD}=5V, R_L=8Ω, Gain = 18dB

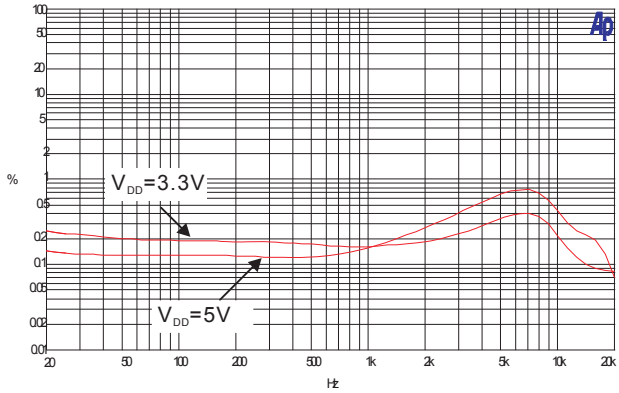


Typical Operating Characteristics (continued)

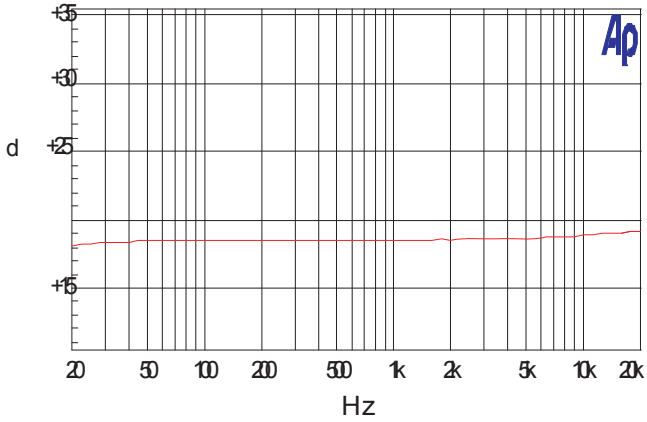
7. THD+N vs. Frequency
Po=0.8W,R_L=4Ω,Gain=18dB



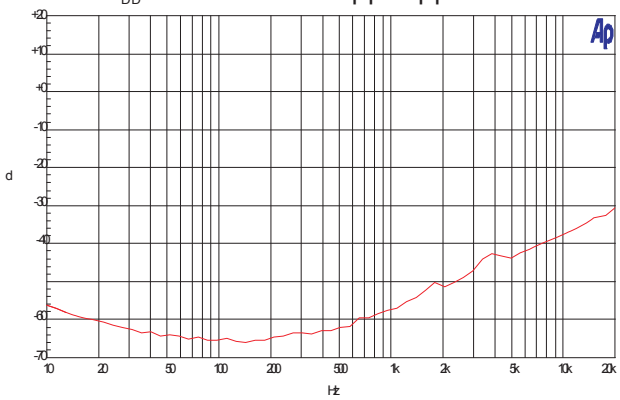
8. THD+N vs. Frequency
Po=0.1W,R_L=8Ω,Gain=18dB



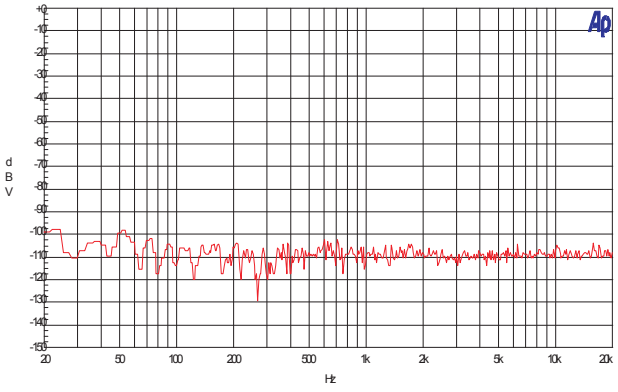
9. Frequency response
V_{DD}=5V, Gain =18dB



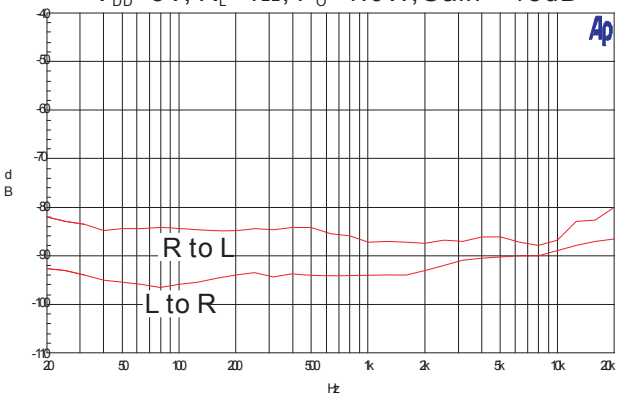
10. Power Supply Ripple Rejection VS Frequency
V_{DD}=5V with 200mVpp Ripple



11. FFT of Noise Output
V_{DD}=5V, Gain = 18dB

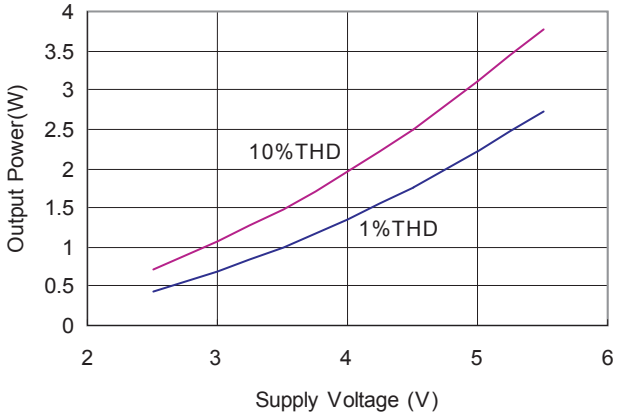


12.Channel Separation
V_{DD}=5V, R_L=4Ω, P_O=1.0W,Gain = 18dB

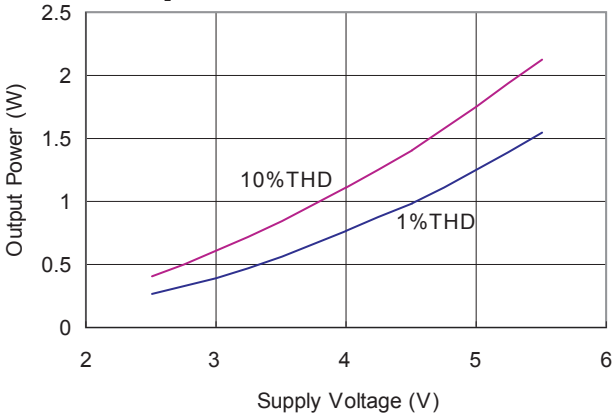


Typical Operating Characteristics (continued)

13. Output Power vs Power Supply
R_L=4Ω



14. Output Power vs Power Supply
R_L=8Ω



Gain Setting (V_{DD}=5V)

Step	Gain (dB)	Step	Gain (dB)	Step	Gain (dB)	Step	Gain (dB)
1	-75.0	17	4.8	33	11.2	49	17.6
2	-39.7	18	5.1	34	11.6	50	18.0
3	-34.0	19	5.5	35	12.0	51	18.4
4	-28.2	20	5.9	36	12.3	52	18.8
5	-22.4	21	6.3	37	12.7	53	19.2
6	-16.5	22	6.7	38	13.2	54	19.6
7	-10.5	23	7.1	39	13.6	55	20.0
8	-8.0	24	7.5	40	14.0	56	20.4
9	-5.5	25	7.9	41	14.4	57	20.9
10	-2.9	26	8.3	42	14.8	58	21.3
11	-0.4	27	8.7	43	15.2	59	21.7
12	1.1	28	9.1	44	15.6	60	22.1
13	2.6*	29	9.6	45	16.0	61	22.5
14	3.6	30	10.0	46	16.4	62	22.9
15	4.0	31	10.4	47	16.8	63	23.4
16	4.4	32	10.7	48	17.2	64	23.8

*Power on gain or gain after reset.
Note: Gain could have 1dB deviation device to device.

Application Notice

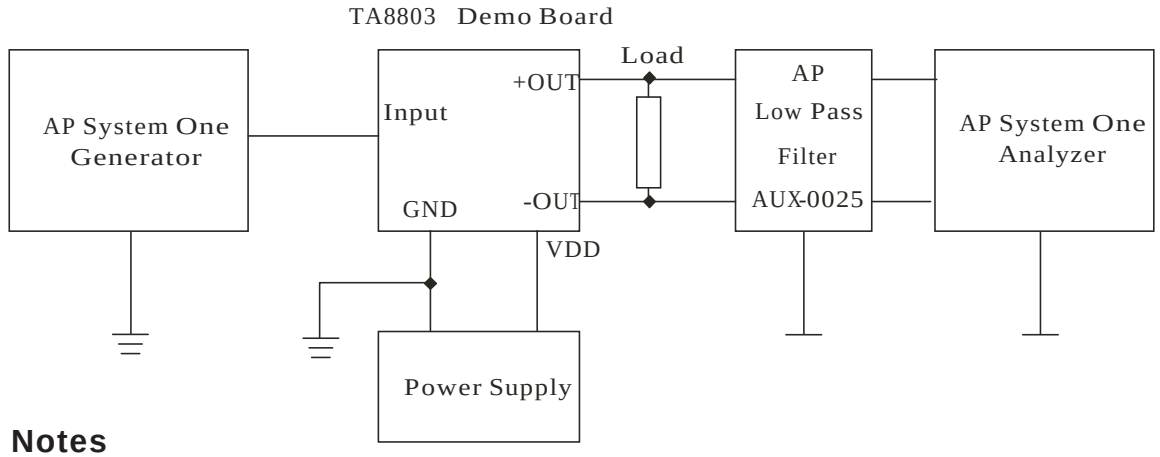
1. When TA8803 works without filter, we must connect the speaker before turn on. Else, it will be easy to damage the chip.

2. When TA8803 works without filter, it will be best that adding a ferrite chip bead at the outgoing line of speaker in order to suppress possible electromagnetic interference .

3. The absolute maximum rating of operation voltage is 6.0V. While using 6V power regulator, even the chip can deliver 4W sine wave with a 4 Ohm speaker, it is not recommended for long term using due to the heat dissipation. But if the input signal is a music signal, then it can work in long term since the average power output is much less than 4W. When using dry battery cell, we should notice that if the battery cell is 4 new dry batteries or alkaline batteries, even the voltage will be over 6V, it still can work safety. Since the output voltage of the 4 pack of new dry batteries will be reduced very quickly after turn on due to the internal resistance of the battery. There is no dangerous of damaging the chip when playing music or speech, even use 4 new dry batteries. To reduce the effect of the increasing of internal resistance of battery after long term discharging, it is recommended to connect a 1000uF electrolytic capacitor between the power supply and the ground.

4. Because digital volume control has big gain, we can not make input signal too high to cause the clipping of the output signal when increase volume, also it may damage the chip.

Test Setup for Performance Testing



Notes

1. The AP AUX-0025 low pass filter is necessary for every class-D amplifier measurement done by AP analyzer.

2. Two 22μH inductors are used in series with load resistor to emulate the small speaker for efficiency and quiescent current measurement.

Application Information

Maximum Gain

As shown in block diagram(page 2),the TA8803 has two internal amplifiers stage. The first stage's gain is externally con figurable, while the second stage's is internally fixed in a fixed-gain, inverting configuration. The closed-loop gain of the first stage is set by selecting the ratio of R_f to R_i while the second stage's gain is fixed at 2x. Consequently, the differential gain for the IC is

$$A_{VD}=20*\log [2*(R_f/R_i)]$$

The TA8803 sets maximum R_f=218kΩ and minimum R_i=27kΩ, thus the maximum closed-gain is 24dB.

Digital Volume Control (DVC)

The TA8803 features a digital volume control which consists of the UP, DN and RST pins. An internal clock is used where the clock frequency value is determined from the following formula:

$$f_{CLK} = f_{OSC} / 2^{13}$$

The oscillator frequency f_{OSC} value is 250kHz typical,with ±20% tolerance.The DVC's clock frequency is 33Hz (cycle time 30ms) typical.

Volume changes are then effected by toggling either the UP or DN pins with a logic low. After a period of 3.5 clocks pulses with either the UP or DN pins held low, the volume will change to the next specified step, either UP or DN, and followed by a short delay. This delay decreases the longer the line is held low, eventually reaching a delay of zero. The delay allows the user to pull the UP or DN terminal low once for one volume change, or hold down to ramp several volume changes. The delay is optimally configured for push button volume control.

If either the UP or DN pin remains low after the first volume transition the volume will change again, but this time after 9.5 clock pulses. The followed transition occurs at 2 clock pulses for each volume transition. This is intended to provide the user with a volume control that pauses briefly after initial application, and then slowly increases the rate of volume change as it is continuously applied. This cycle is shown in the timing diagram shown in figure 1.

There are 64 discrete gain settings ranging from +24dB maximum to -75dB minimum. Upon device power on or applied a logic low to the RST pin, the amplifier's gain is set to a default value of -4.5dB. However, when coming out of mute mode, the TA8803 will revert back to its previous gain setting. Volume levels for each step vary and are specified in Gain Setting table on page 7.

If both the UP and DN pins are held high, no volume change will occur. Trigger points for the UP and DN pins are at 70% of V_{DD} minimum for a logic high, and 20% of V_{DD} maximum for a logic low. It is recommended, however, to toggle UP and DN between V_{DD} and GND for best performance.

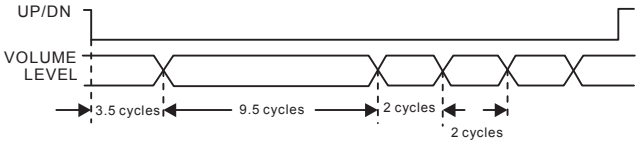


Figure 1.Timming Diagram

Mute Operation

The $\overline{\text{MUTE}}$ pin is an input for controlling the output state of the TA8803 . A logic low on this pin disables the outputs, and a logic high on this pin enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade. Quiescent current is listed in the electrical characteristic table. The $\overline{\text{MUTE}}$ pin can be left floating due to the pull-up internal.

Shutdown operation

In order to reduce power consumption while not in use, the TA8803 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{\text{SHDN}}$ pin. By switching the $\overline{\text{SHDN}}$ pin connected to GND, the TA8803 supply current draw will be minimized in idle mode. The $\overline{\text{SHDN}}$ pin cannot be left floating due to the pull-down internal.

Power supply decoupling

The TA8803 is a high performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output THD and PSRR are as low as possible. Power supply decoupling is affecting low frequency response. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1.0μF, placed as close as possible to the device V_{DD} terminal works best. For filtering lower-frequency noise signals, a larger capacitor of 10μF (ceramic) or greater placed near the audio power amplifier is recommended.

Input Capacitor (C_i)

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is needed to couple in low frequencies without severe attenu ation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system perfor mance. In this case, input capacitor (C_i) and input resistance (R_i) of the amplifier form a high-pass filter with the corner frequency determined equation below,

$$f_C=\frac{1}{2\pi R_i C_i}$$

In addition to system cost and size, click and pop perfor mance is affected by the size of the input coupling capacitor, C_i. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the internal circuit via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Analog Reference Bypass Capacitor (C_{BYP})

The Analog Reference Bypass Capacitor (C_{BYP}) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor (C_{BYP}) values of 0.47μF to 1.0μF ceramic is recommended for the best THD and noise performance. Increasing the bypass capacitor reduces clicking and popping noise from power on/off and entering and leaving shutdown.

Under Voltage Lock-out (UVLO)

The TA8803 incorporates circuitry designed to detect when the supply voltage is low. When the supply voltage drops to 1.85V or below, the TA8803 outputs are disable, and the device comes out of this state and starts to normal functional when the supply voltage increases.

Short Circuit Protection (SCP)

The TA8803 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output and output-to-GND short. When a short circuit is detected on the outputs, the outputs are disable immediately. If the short was removed, the device activates again.

Over Temperature Protection

Thermal protection on the TA8803 prevents damage to the device when the internal die temperature exceeds 150°C. There is a 15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 60°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

How to Reduce EMI (Electro Magnetic Interference)

A simple solution is to put an additional capacitor 1000uF at power supply terminal for power line coupling if the traces from amplifier to speakers are short (<20cm).

Most applications require a ferrite bead filter which shows at Figure 3. The ferrite filter reduces EMI around 1 MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

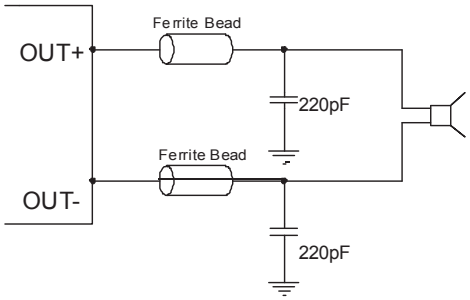


Figure 3: Ferrite Bead Filter to reduce EMI

PCB Layout Guidelines

Grounding

At this stage it is paramount that we acknowledge the need for separate grounds. Noise currents in the output power stage need to be returned to output noise ground and nowhere else. Were these currents to circulate elsewhere, they may get into the power supply, the signal ground, etc, worse yet, they may form a loop and radiate noise. Any of these instances results in degraded amplifier performance. The logical returns for the output noise currents associated with Class D switching are the respective PGND pins for each channel. The switch state diagram illustrates that PGND is instrumental in nearly every switch state. This is the perfect point to which the output noise ground trace should return. Also note that output noise ground is channel specific. A two channels amplifier has two mutually exclusive channels and consequently must have two mutually exclusive output noise ground traces. The layout of the TA8803 offers separate PGND connections for each channel and in some cases each side of the bridge. Output noise grounds must tie to system ground at the power in exclusively. Signal currents for the inputs, reference, etc need to be

the signal components and the GND pin. GND then ties to system ground.

Power Supply Line

As same to the ground, VDD and each channel PVDD need to be separated and tied together at the system power supply. Recommend that all the trace could be routed as short and thick as possible. For the power line layout, just imagine water stream, any barricade placed in the trace (shows in figure 4) could result in the bad performance of the amplifier.

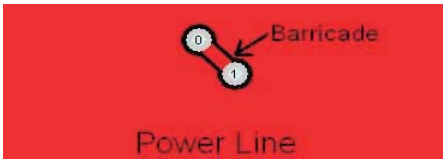
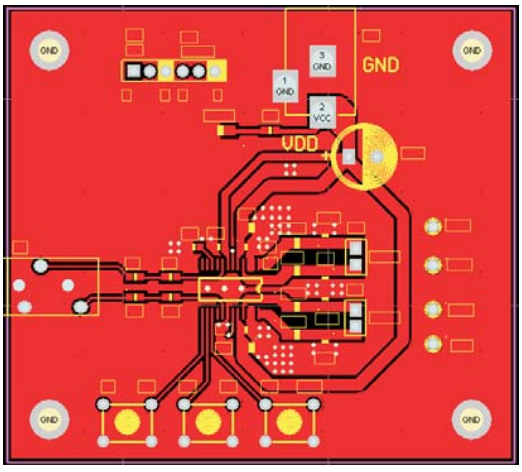


Figure 4

Components Placement

The power supply decoupling capacitors need to be placed as close to VDD and PVDD pins as possible. The inputs need to be routed away from the noisy trace. The VREF bypass capacitor also needs to be close to the pin of IC very much.

PCB Top Layer



PCB Bottom Layer

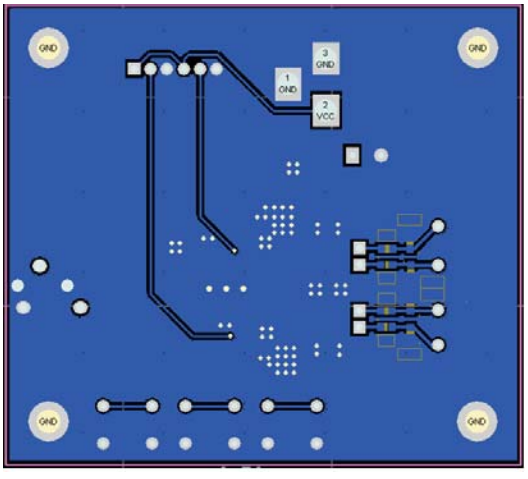
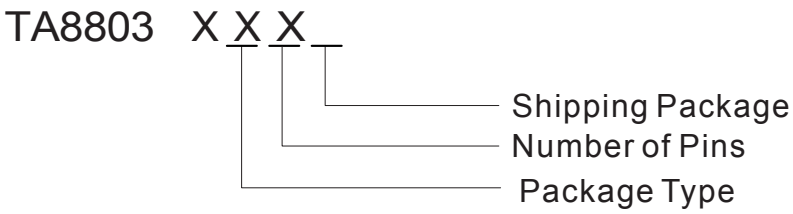


Figure 5: Layout Example

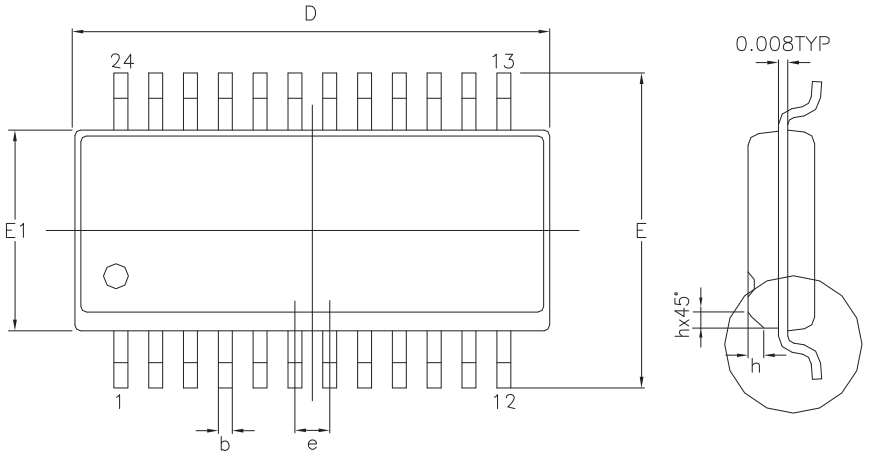
Ordering Information

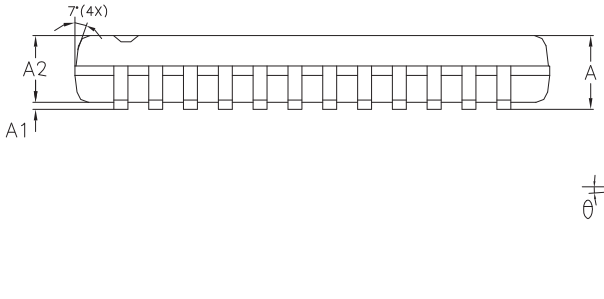


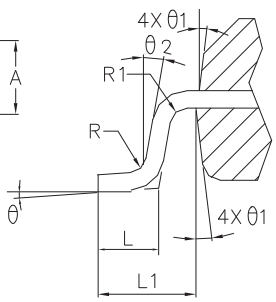
Part Number	Marking	Package Type	Shipping Package
TA8803NHR	TA8803 XXXYWWLL	SSOP-24	2,500 Units/Tape & Reel

Outline Dimension

SSOP-24







SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.061	0.069
A1	0.004	–	0.010
A2	0.049	0.057	0.065
b	0.008	0.010	0.012
D	0.335	0.341	0.347
E	0.228	0.236	0.244
E1	0.150	0.154	0.158
e	–	0.025	–
L	0.016	0.033	0.050
L1	0.041 REF		
R	0.003	–	–
R1	0.003	–	–
h	0.010	0.015	0.020
θ	0°	4°	8°
θ1	5°	10°	15°
θ2	0°	–	–

UNIT : INCH