单电源四通道缓冲转换门器件，具有三态CMOS输出的电平转换器

Single Power Supply Quadruple Buffer Translator GATE With 3-State Output CMOS Logic Level Shifter

■ FEATURES

- Single-Supply Voltage Translator at 5.0-V, 3.3-V, 2.5-V, and 1.8-V V_{CC}
- Operating Range of 1.8 V to 5.5 V
- Up Translation
  - 1.2 V to 1.8 V at 1.8-V V_{CC}
  - 1.5 V to 2.5 V at 2.5-V V_{CC}
  - 1.8 V to 3.3 V at 3.3-V V_{CC}
  - 3.3 V to 5.0 V at 5.0-V V_{CC}
- Down Translation
  - 3.3 V to 1.8 V at 1.8-V V_{CC}
  - 3.3 V to 2.5 V at 2.5-V V_{CC}
  - 5.0 V to 3.3 V at 3.3-V V_{CC}
- Logic Output is Referenced to V_{CC}
- Characterized up to 50 MHz at 3.3-V V_{CC}
- 5.5 V Tolerance on Input Pins
- -40°C to 125°C Operating Temperature Range
- Pb-Free Packages Available: QFN14L-3.5×3.5
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- Supports Standard Logic Pinouts

- 单电源电压转换
- 1.8V至5.5V 的工作电压范围
- 上行转换模式
  - 1.8V V_{CC}时，1.2V至1.8V
  - 2.5V V_{CC}时，1.5V至2.5V
  - 3.3V V_{CC}时，1.8V 至 3.3V
  - 5.0V V_{CC}时，3.3V 至 5.0V
- 下行转换模式
  - 1.8V V_{CC}时，3.3V至1.8V
  - 2.5V V_{CC}时，3.3V至2.5V
  - 3.3V V_{CC}时，5.0V 至 3.3V
- 逻辑输出以电源V_{CC}为基准
- 3.3V V_{CC}时，特有高达50MHz的频率
- 输入端子上的TTL兼容性
- 任一有效V_{CC}上的输入可耐受5.5V 电压
- -40°C 至125°C 工作温度范围
- 采用无铅封装：QFN14L-3.5×3.5
- 锁断性能超过250mA，符合JESD 17 规范
- 静电放电(ESD) 性能测试符合JESD 22 规范
  - 2000V 人体模型（A114-B，II 类）
  - 200V 机器模型(A115-A)
  - 1000V 充电器件模型(C101)
- 实现标准门功能和插槽替换

■ APPLICATIONS

- Tablet
- Smartphone
- Personal Computer
- Industrial Automotive

- 平板电脑
- 智能手机
- 个人计算机
- 工业汽车应用

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■ DESCRIPTION

HT4125 is a low-voltage CMOS buffer gate that operates at a wider voltage range for portable, telecom, industrial, and automotive applications. The output level is referenced to the supply voltage and is able to support 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

The input is designed with a lower threshold circuit to match 1.8-V input logic at VCC = 3.3 V and can be used in 1.8 V to 3.3 V level-up translation. In addition the 5-V tolerant input pins enable down translation (for example, 3.3 V to 2.5 V output at VCC = 2.5 V). The wide VCC range of 1.8 V to 5.5 V allows the generation of desired output levels to connect to controllers or processors.

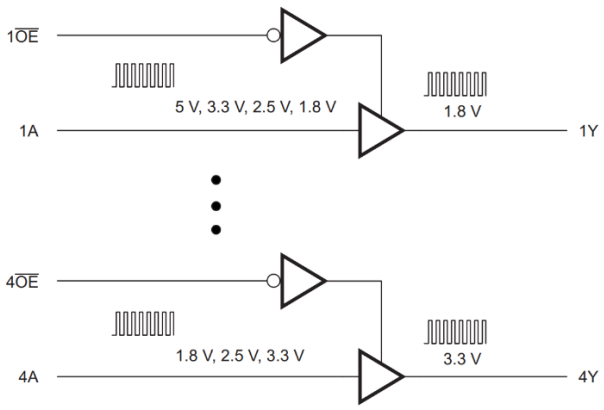
The HT4125 device is designed with current-drive capability of 8 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

HT4125 是一款低压CMOS 缓冲门器件，可运行在针对便携式和电池设备的更宽电压范围内。

其采用了较低阀值电路来设计此输入，以便匹配Vcc =3.3V 时的1.8V 输入逻辑，并且可被用在1.8V 至3.3V 电平上行转换器功能中。此外，输入端子上的5V 输入耐受可在Vcc = 2.5V 时将芯片配置为3.3V 至2.5V 输出的下行转换。1.8 至5.5V 的宽Vcc 范围有可能实现所需的开关输出电平连接至控制器或处理器。

HT4125 被设计成具有8mA 的经优化电流驱动能力，以减少由高驱动输出导致的线路反射、过冲和下冲。

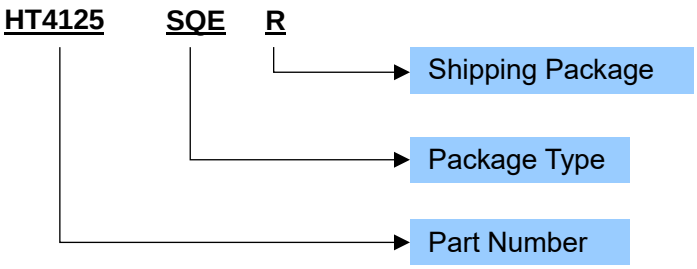
■ SIMPLIFIED APPLICATION DIAGRAM



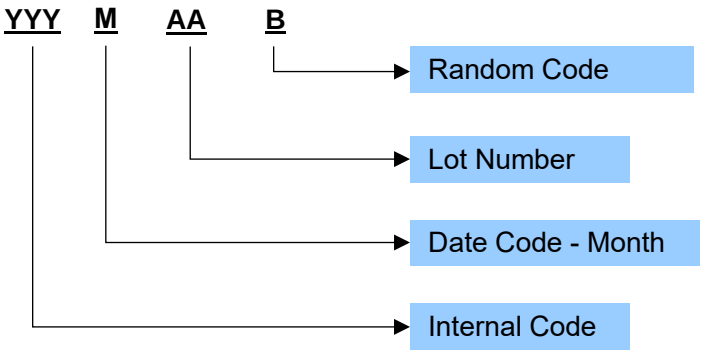
■ ORDERING INFORMATION

Ordering Number	Package Type	Marking	Operating Temperature Range	Shipping Package / MOQ
HT4125SQER	QFN14L-3.5×3.5	HT4125SQ YYYMAAB[1]	-40℃～125℃	Tape and Reel / 5000pcs

Ordering Number

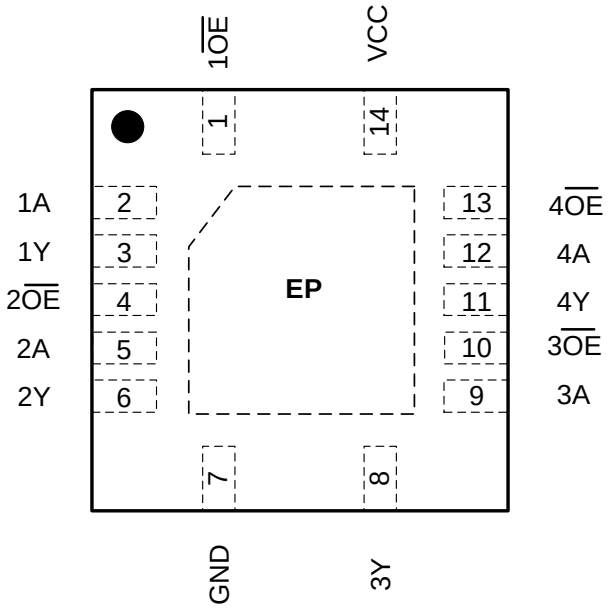


Production Tracking Code



[1] YYYMAAB is production tracking code

■ TERMINAL CONFIGURATION



■ TERMINAL FUNCTION

Terminal No.	Name	I/O	Description
1	1 $\overline{OE}$	I	Enable 1.
2	1A	I	Input 1.
3	1Y	O	Output 1
4	2 $\overline{OE}$	I	Enable 2
5	2A	I	Input 2
6	2Y	O	Output 2
7	GND	-	Ground
8	3Y	O	Output 3
9	3A	I	Input 3
10	3 $\overline{OE}$	I	Enable 3
11	4Y	O	Output 4
12	4A	I	Input 4
13	4 $\overline{OE}$	I	Enable 4
14	V_{CC}	-	Power in
EP	Exposed Thermal Pad	-	No connection, connect to ground.

■ SPECIFICATIONS[1]

● Absolute Maximum Ratings [2]

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Supply voltage range	VCC	-0.5		7.0	V
Input voltage range[3]	V_I	-0.5		7.0	V
Voltage range applied to any output in the high-impedance or power-off state	V_O	-0.5		4.6	V
Voltage range applied to any output in the high or low state		-0.5		V_{CC} + 0.5	V
Input clamp current, VI < 0	I_{IK}			－20	mA
Input clamp current, V_O < 0 or V_O > VCC	I_{OK}			±50	mA
Continuous output current	I_O			±35	mA
Continuous current through VCC or GND				±70	mA
Storage Temperature	T_{STG}	-65		150	℃
ESD (HBM)			2		kV
ESD (CDM)			1		kV

● Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise specified.

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage	VCC		1.6		5.5	V
Input voltage	V_I		0		5.5	V
Output voltage	V_O	High or low state	0		VCC	V
		Hi-Z	0		VCC	V
High-level output current	I_{OH}	VCC = 1.8 V			-3	mA
		VCC = 2.5 V			-6	
		VCC = 3.3 V			-8	
		VCC = 5.0 V			-16	
Low-level output current	I_{OL}	VCC = 1.8 V			3	mA
		VCC = 2.5 V			5	
		VCC = 3.3 V			8	
		VCC = 5.0 V			16	
Input transition rise or fall rate	Δt/Δv	VCC = 1.6 V to 2.0 V			20	ns/V
		VCC = 2.3 V to 2.7 V			20	
		VCC = 3 V or 3.6 V			20	
		VCC = 4.5 V to 5.0 V			20	
Operating free-air temperature	T_A		-40		125	℃

● Thermal Information

PARAMETER	Symbol	TYP	UNIT
Junction-to-ambient thermal resistance	$R_{\theta JA}$	52.9	℃/W
Junction-to-case (top) thermal resistance	$R_{\theta JCtop}$	67.8	
Junction-to-board thermal resistance	$R_{\theta JB}$	29.0	
Junction-to-top characterization parameter	ψ_{JT}	2.6	
Junction-to-board characterization parameter	ψ_{JB}	29.1	
Junction-to-case (bottom) thermal resistance	$R_{\theta JCbot}$	9.3	

[1] Depending on parts and PCB layout, characteristics may be changed.

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

[3] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

● Electrical Characteristics

Over operating free-air temperature range, unless otherwise specified.

PARAMETER	Symbol	Condition	VCC	T_A = 25℃			T_A = -40 to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	
High-level input voltage	V_{IH}		1.65V to 1.9V	0.95			1		V
			2.3V to 2.7V	1.1			1.2		
			3V to 3.6V	1.3			1.35		
			4.5V to 5.0V	2			2		
Low-level input voltage	V_{IL}		1.65V to 1.9V			0.55		0.5	V
			2.3V to 2.7V			0.7		0.6	
			3V to 3.6V			0.85		0.75	
			4.5V to 5.0V			0.9		0.85	
High-level output voltage	V_{OH}	I_{OH} = -50μA	1.65V to 5.5V	V_{CC}-0.1			V_{CC}-0.1		V
		I_{OH} = -2mA	1.65V	1.4			1.35		V
		I_{OH} = -3mA	2.3V	2.05			2.0		V
		I_{OH} = -5mA	3.0V	2.7			2.6		V
		I_{OH} = -8mA		2.6			2.5		
		I_{OH} = -8mA	4.5V	3.7			3.6		V
		I_{OH} = -16mA		3.8			3.7		
		I_{OH} = -16mA	5.0V	4.4			4.3		V
Low-level output voltage	V_{OL}	I_{OL} = 50μA	1.65 V to 5.5 V			0.1		0.1	V
		I_{OL} = 2mA	1.65V			0.1		0.1	V
			1.8 V			0.2		0.3	
		I_{OL} = 3mA	2.3 V			0.2		0.3	V
			2.5 V			0.25		0.3	
		I_{OL} = 5mA	3.0 V			0.35		0.4	V
		I_{OL} = 8mA				0.4		0.45	
		I_{OL} = 8mA	3.3 V			0.45		0.5	V
		I_{OL} = 8mA	4.5 V			0.50		0.55	V
		I_{OL} = 16mA				0.55		0.55	
		I_{OL} = 16mA	5.0 V			0.55		0.55	V
Input current	I_I	V_I =0 V or VCC	0V, 1.8V, 2.5V, 3.3V, 5.5V			±0.1		±1	μA
VCC current consumption	I_{CC}	V_I =0 V or VCC, I_O = 0, open on loading	5.0V			2		20	μA
			3.3V			2		20	
			2.5V			2		20	
			1.8V			2		20	
VCC current consumption	Δ I_{CC}	One input at 0.3 V or 3.4 V Other inputs at 0 or VCC, I_O = 0	5.5V			1.35		1.5	μA
		One input at 0.3 V or 1.1 V Other inputs at 0 or VCC, I_O = 0	1.8V						
Output current in the high-impedance state	I_{OZ}	V_O = V_{CC} or GND	5.5V			±0.25		±2.5	μA
Output current in power-off state	I_{off}	V_O or V_I = 0 to 5.5 V	0V			0.5		5	μA
Input capacitance	C_I	V_O = Vcc or GND	3.3V		1.6		1.6		pF
Output capacitance	C_O	V_O = Vcc or GND	3.3V		4.8		4.8		pF

● Timing Requirements

Over operating free-air temperature range, unless otherwise specified. (See Figure 2)

PARAMETER	FROM (INPUT)	TO(OUTPUT)	FREQUENCY (TYP)	VCC	C_L	T_A = 25℃			T_A = -40 to 125℃			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Any In	Y	DC to 50MHz	5.0V	15pF		2.8	3.2		3	3.5	ns
					30pF		3	3.5		3	4.5	
				3.3V	15pF		4	4.5		5	5.5	
					30pF		5	5.5		5.5	6.5	
				2.5V	15pF		5.5	6.5		7	7.5	
					30pF		6.5	7		7.5	8.5	
			DC to 30MHz	1.8V	15pF		10	11		11	12	
					30pF		11	12		12.5	13	
t_{PZH}	$\overline{OE}$	Y	DC to 50MHz	5.0V	15pF		3.5	4		3.5	4	ns
					30pF		3.8	4.2		4	4.5	
				3.3V	15pF		5	5.8		5.8	6.1	
					30pF		5.5	6		5.7	6.5	
				2.5V	15pF		7.5	8		8.5	9	
					30pF		8	8.5		9	9.5	
			DC to 30MHz	1.8V	15pF		14.5	15		15.5	16.5	
					30pF		15.5	16		16	17	
t_{PZL}	$\overline{OE}$	Y	DC to 50MHz	5.0V	15pF		3	3.5		3.5	4	ns
					30pF		3.5	4		4	4.5	
				3.3V	15pF		5.3	5.6		6	6.2	
					30pF		5.8	6.2		7	7.5	
				2.5V	15pF		8	8.5		9	9.5	
					30pF		9	9.5		10.5	11	
			DC to 30MHz	1.8V	15pF		17	17.5		18	18.5	
					30pF		18	18.5		19	20	
t_{PHZ}	$\overline{OE}$	Y	DC to 50MHz	5.0V	15pF		3	3.5		3.5	4	ns
					30pF		3.5	4		4	4.5	
				3.3V	15pF		3.5	4		4.5	5	
					30pF		5	6		6.5	7	
				2.5V	15pF		5.5	6		6	6.5	
					30pF		7.6	8		8	9	
			DC to 30MHz	1.8V	15pF		7.5	8		8	8.5	
					30pF		11	12		12	13	
t_{PLZ}	$\overline{OE}$	Y	DC to 50MHz	5.0V	15pF		2	2.5		2	2.7	ns
					30pF		2	3		2	3.2	
				3.3V	15pF		2.3	2.8		2.5	3.2	
					30pF		2.8	3.2		3.3	4	
				2.5V	15pF		3.3	3.8		3.8	4.2	
					30pF		4	4.3		4.2	5	
			DC to 30MHz	1.8V	15pF		5	5.5		5	5.7	
					30pF		6.5	7		7	8.5	
t_{sk}	Any In	Y	DC to 50MHz	5.0V to 2.5V	15pF				1		1	ns
			DC to 30MHz	1.8V	15pF							

● Noise Characteristics

VCC = 3.3V, C_L = 50pF, TA = 25℃.

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$		0.4	0.8	V
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$		-0.3	-0.8	V
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$		3		V
High-level dynamic input voltage	$V_{IH(D)}$	2.31			V
Low-level dynamic input voltage	$V_{IL(D)}$			0.99	V

● Operating Characteristics

VCC = 5V, TA = 25℃.

PARAMETER	Symbol	Condition	MAX	UNIT
Power dissipation capacitance	C_{pd}	C_L = 50 pF, f = 10 MHz	16	pF

● Typical Characteristics

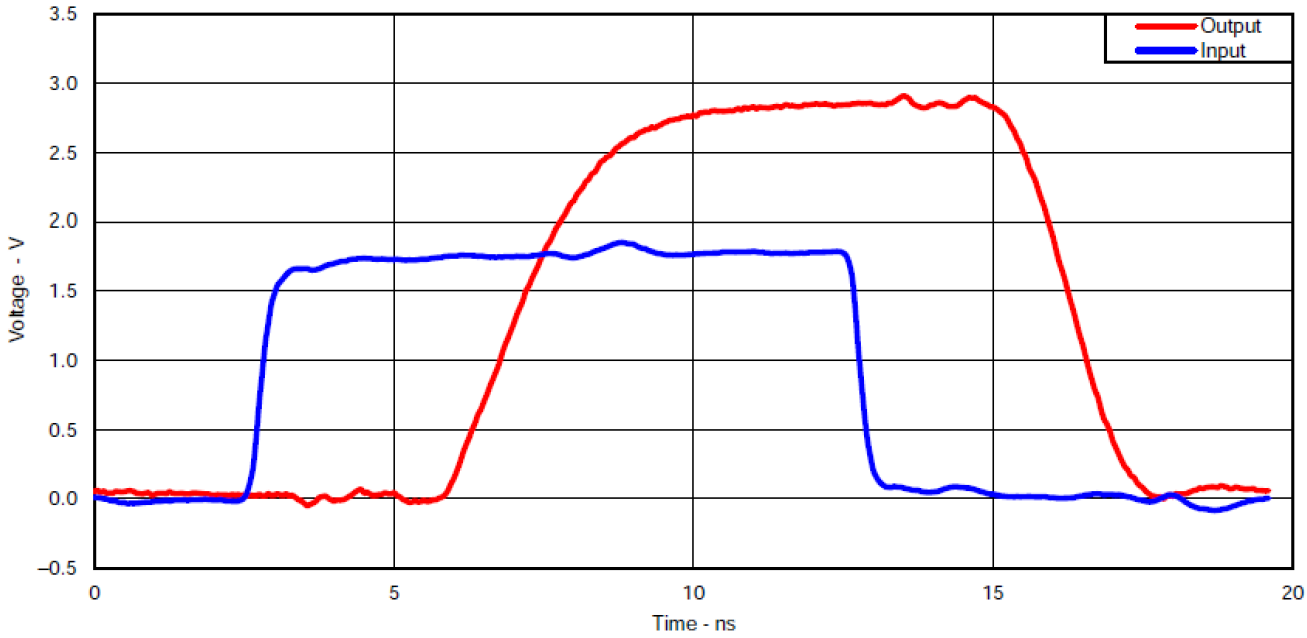


Figure 1 Switching Characteristics at 50MHz

■ Parameter Measurement Information

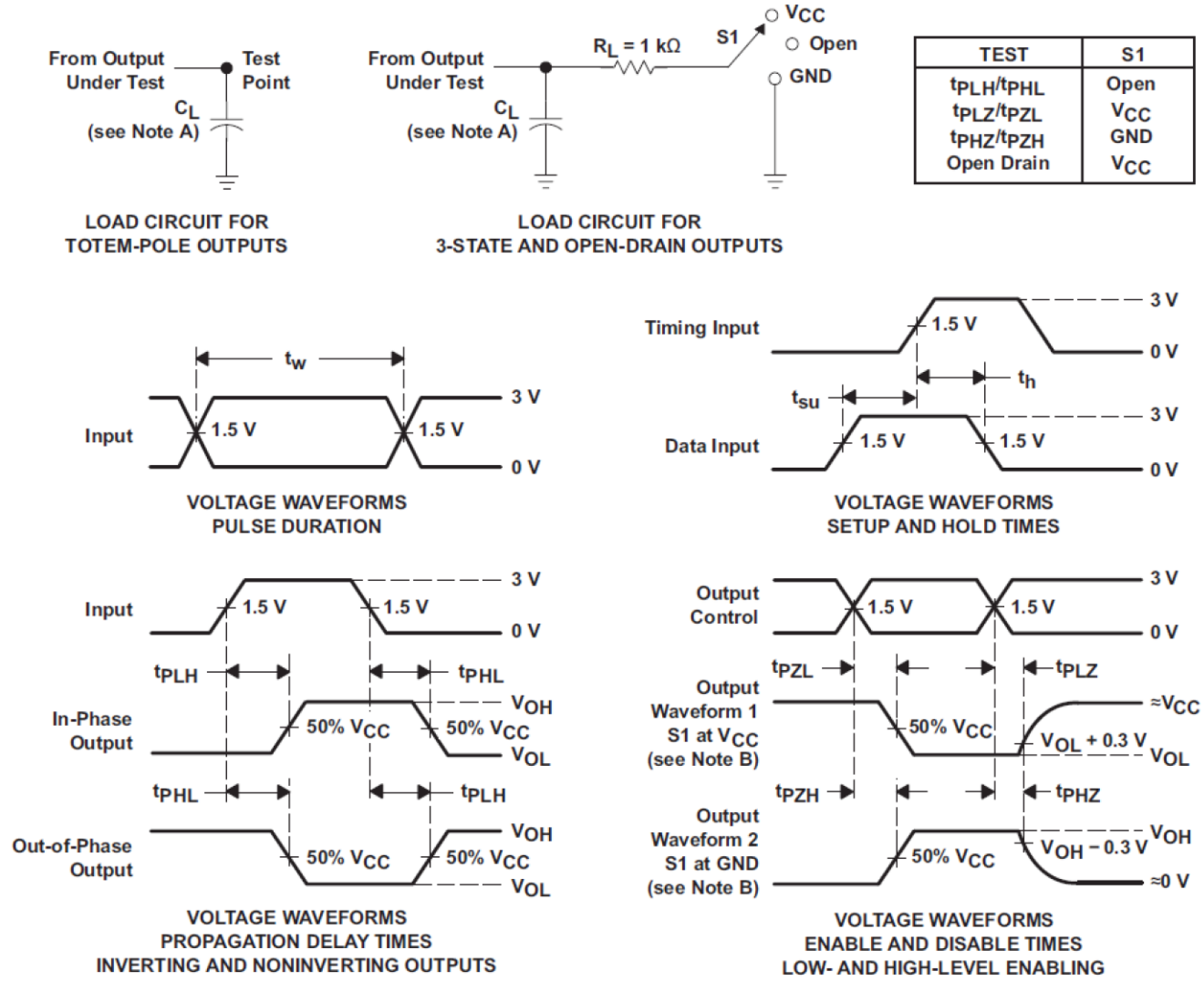


Figure 2 Load Circuit and Voltage Waveforms

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR <1 MHz, Z_O = 50Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

■ DEAILED DESCRIPTION

1 Overview

HT4125 was created to allow up- or down-voltage translation with only one power rail. It has over-voltage tolerant inputs that allow down translation from up to 5.5 V to the VCC level that can be as low as 1.8 V. HT4125 also has a lowered switching threshold that allows it to translate up to the VCC level that can be as high as 5.5 V.

HT4125 仅需要提供一个电源，即可支持上行或者下行的电平转换。在进行下行电平转换时，输入电平最高可达 5.5V, VCC 电压则可低至 1.8V。在进行上行电平转换时，HT4125 支持更低的输入切换电平，VCC 最高电压可达 5.5V。

1.1 Translating Down

Using HT4125 to translate down is very simple. Because the inputs are tolerant to 5.5 V at any valid VCC, HT4125 can be used to down translate. The input can be any level above VCC up to 5.5 V and the output will equal the VCC level, which can be as low as 1.8 V. One important advantage to down translating using this part is that the ICC current will remain less than or equal to the specified value.

Down translation possibilities with HT4125:

With 1.8-V VCC from 2.5 V, 3.3 V, or 5 V down to 1.8 V;

With 2.5-V VCC from 3.3 V or 5 V down to 2.5 V.

With 3.3-V VCC from 5 V down to 3.3 V.

使用HT4125进行下行电平转换时，输入电平可高于VCC，输出电平则是VCC，VCC最高5.5V，最低1.8V。下行电平转换时，HT4125的ICC电流不会操作给定的最大值。

几种可能的下行电平转换应用：

1.8V VCC，输入 2.5V, 3.3V 或 5V 电平，输出 1.8V 电平；

2.5V VCC，输入 3.3V 或 5V 电平，输出 2.5V 电平；

3.3V VCC，输入 5V 电平，输出 3.3V 电平。

1.2 Translating Up

Using HT4125 to translate up is very simple. The input switching threshold is lowered so the high level of the input voltage can be much lower than a typical CMOS V_{IH}.

Up translation possibilities with HT4125:

With 2.5-V VCC from 1.8 V to 2.5 V.

With 3.3-V VCC from 1.8 V or 2.5 V to 3.3 V.

With 5-V VCC From 2.5 V or 3.3 V to 5 V.

使用 HT4125 进行下行电平转换时，输入电平可低于 CMOS 典型的 V_{IH}。

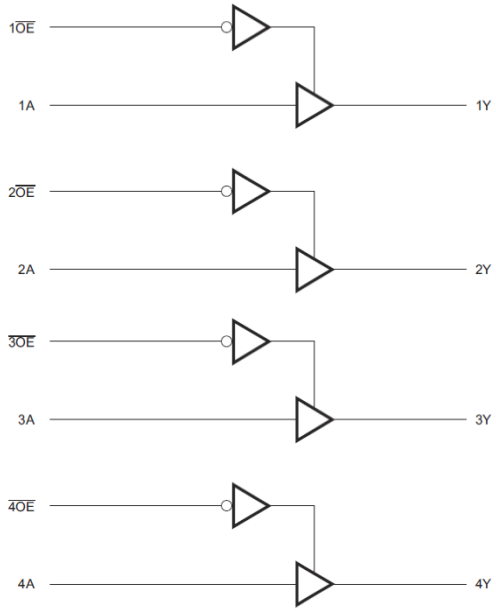
几种可能的上行电平转换应用：

2.5V VCC，输入 1.8V、输出 2.5V 电平；

3.3V VCC，输入 1.8V 或 2.5V、输出 3.3V 电平；

5V VCC，输入 2.5V 或 3.3V 电平，输出 5V 电平。

2 Functional Block Diagram



3 Feature Description

This part is a single supply buffer that is capable up or down translation. The output will equal VCC while the input can vary from 1.2 V to 5.5 V.

Up Translation Mode:

1.2 V to 1.8 V at 1.8-V VCC;

1.5 V to 2.5 V at 2.5-V VCC;

1.8 V to 3.3 V at 3.3-V VCC;

3.3 V to 5.0 V at 5.0-V VCC.

Down Translation Mode:

3.3 V to 1.8 V at 1.8-V VCC;

3.3 V to 2.5 V at 2.5-V VCC;

5.0 V to 3.3 V at 3.3-V VCC.

HT4125 是一个单电源缓冲器，可支持上行或者下行的电平转换。其输出电平即为 VCC，输入电平支持 1.2V 到 5.5V。

上行转换模式：

1.8V VCC, 1.2V 转至 1.8V;

2.5V VCC, 1.5V 转至 2.5V;

3.3V VCC, 1.8V 转至 3.3V;

5.0V VCC, 3.3V 转至 5.0V.

下行转换模式：

1.8V VCC, 3.3V 转至 1.8V;

2.5V VCC, 3.3V 转至 2.5V;

3.3V VCC, 5.0V 转至 3.3V。

4 Device Functional Modes

This device performs the function of a buffer where input logic level equals the output logic level, while providing buffering and drive to the output. The device will also translate voltages up or down while performing this function.

HT4125 为一个缓冲器，同时可作为电平转换，并驱动输出。

Table 1 Function Table

Inputs		**Output Y**
$\overline{OE}$	**A**	
L	H	H
L	L	L
H	X	Z

Table 2 Supply VCC = 3.3V

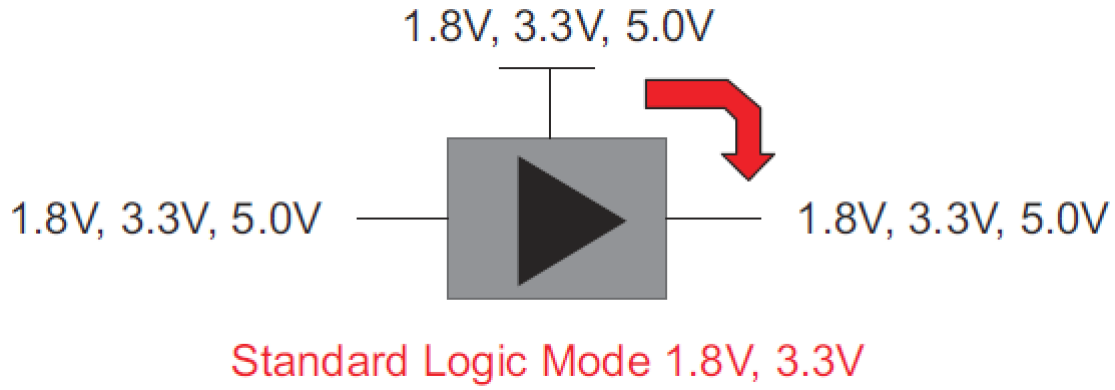
Input **(Lower Level Input)**	**Output** **(VCC CMOS)**
A	H
V_{IH}(min) = 1.35V	V_{OH}(min) = 2.9V
V_{IL}(max) = 0.8V	V_{OL}(max) = 0.2V

■ APPLICATIONS AND IMPLEMENTATION

1 Application Information

Based upon the lower-threshold circuit design of the device, the device also supports level translation. For level translation up and down, the device requires only a single power supply.

HT4125 支持更低的切换电平，可作为电平转换，仅需一个供电电源。



2 Typical Application

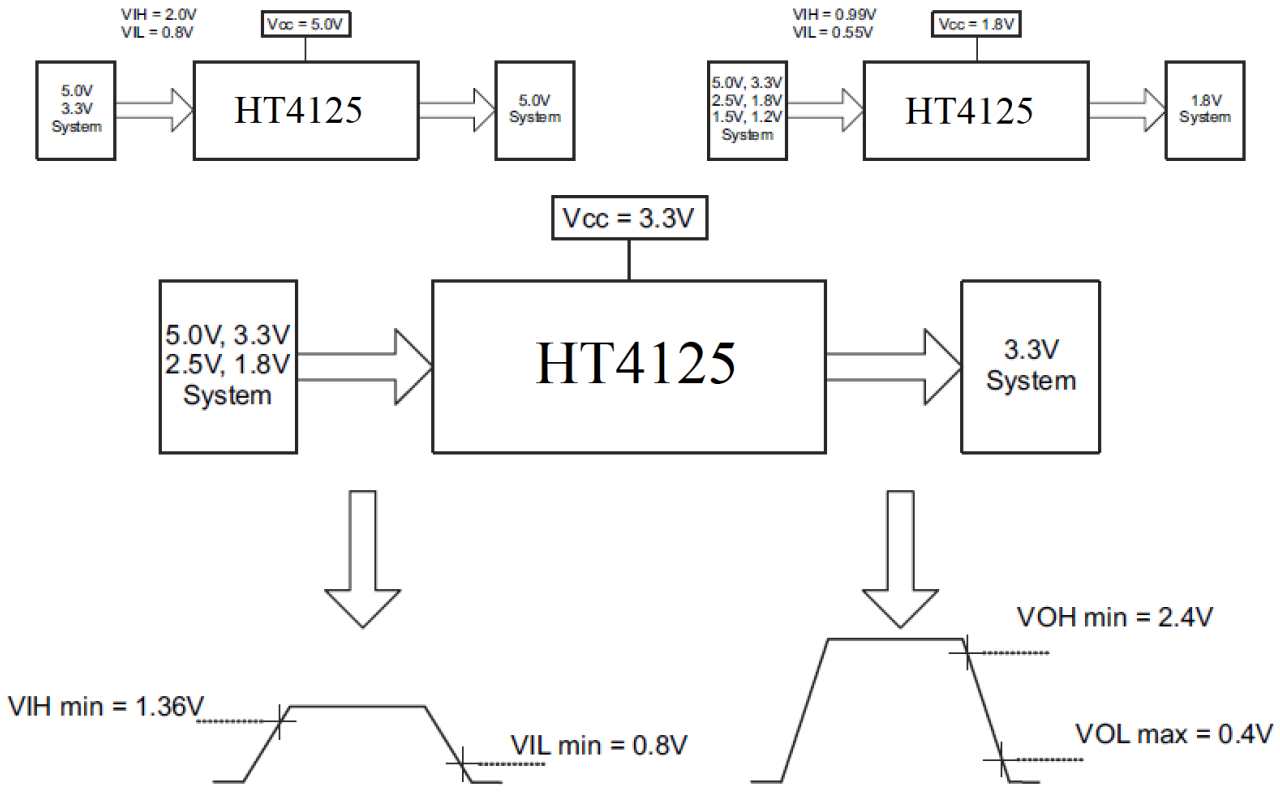


Figure 3 Switching Thresholds for 1.8V to 3.3V Translation

2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. The input threshold levels are lowered to allow for up translation. At 5 V the device has equivalent TTL input levels.

HT4125 采用了 CMOS 技术，具有输出驱动能力，在上行电平转换时支持更低的输入切换电平，5V 供电时具有类似 TTL 的输入电平范围。

2.2 Detailed Design Procedure

2.2.1 Recommended input conditions

- Rise time and fall time specifications. See (Δt/ΔV) in Recommended Operating Conditions table.

上升时间和下降时间参数。参见 Recommended Operating Conditions 表格。

- Specified high and low levels. See (V_{IH} and V_{IL}) in Electrical Characteristics.

高电平和低电平参数。参见 Electrical Characteristics 表格。

- Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid VCC.

输入最高电平可达 5.5V。

2.2.2 Recommended output conditions

- Load currents should not exceed 35 mA per output and 70 mA total for the part.

输出负载电流，每个通道输出不能超过 35mA，总计不能超过 70mA。

- Outputs should not be pulled above VCC.

输出不能上拉超过 VCC 的电压。

2.3 Application Curves

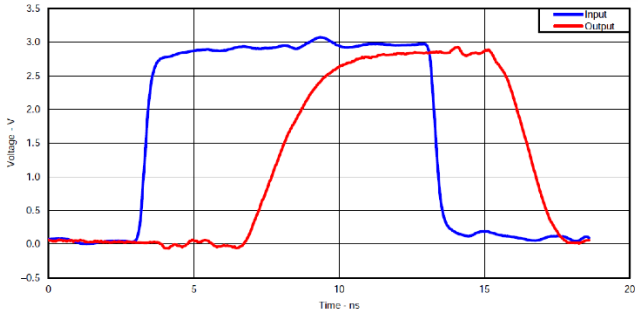


Figure 4 Switching Characteristics at 50 MHz (3.3 V to 3.3 V at 3.3-V VCC)

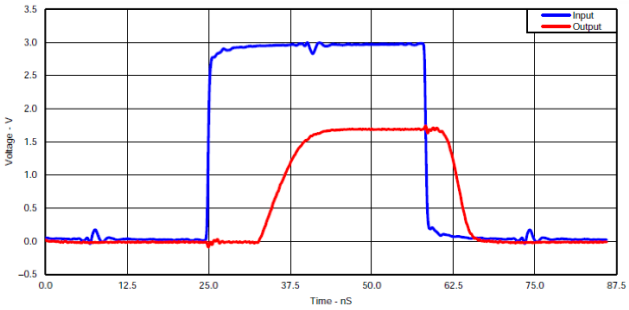


Figure 5 Switching Characteristics at 15 MHz (3.3 V to 1.8 V at 1.8-V VCC)

3 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the Recommended Operating Conditions.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple VCC pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

HT4125的电源供电可介于Recommended Operating Conditions表格中Min和Max中的任意值。VCC引脚应有良好的滤波电容，一般一个0.1 μF即可，也可使用多组并联电容滤波，如0.1 μF和1 μF。滤波电容应尽可能靠近引脚放置。

4 Layout

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Figure 6 are the rules that must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC whichever make more sense or is more convenient.

It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they also cannot float when disabled.

当使用 HT4125 这类多通道逻辑器件时，输入端不应悬空，而是设置成如下图的方式。

不使用的输出则一般可以悬空。

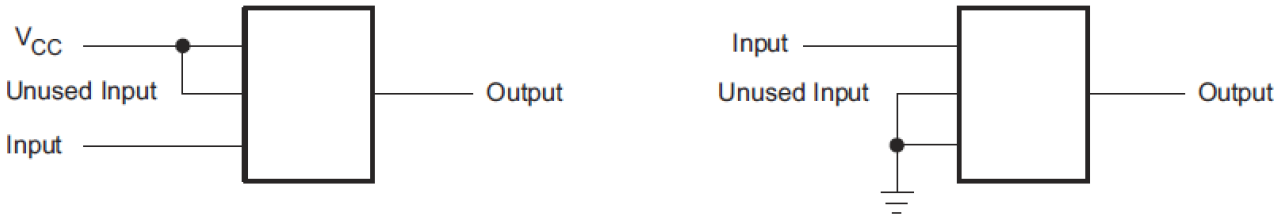
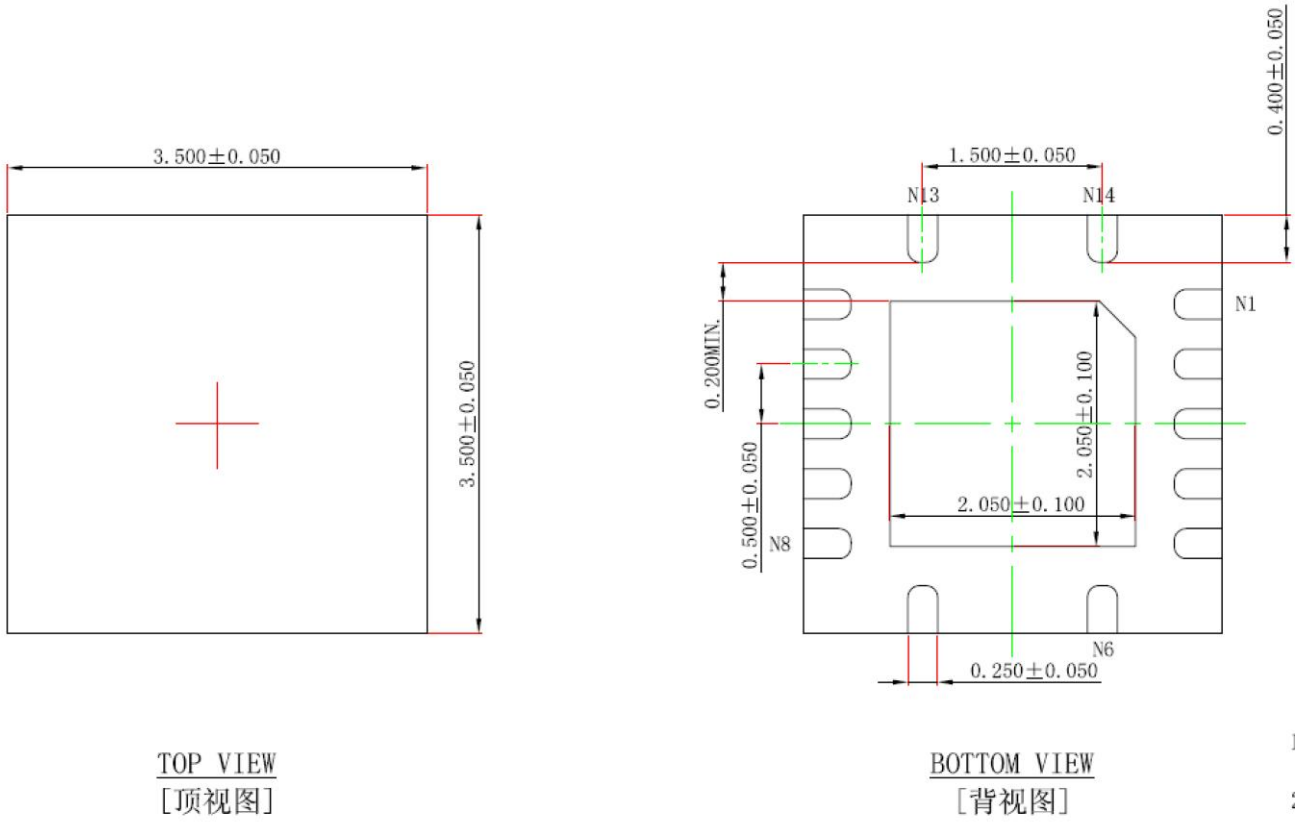


Figure 6 Layout Diagram

■ PACKAGE OUTLINE

SQE (QFN14L-3.5×3.5), Dimensions in Millimeters



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.700	0.800